Workshop on Architecture of Smart Camera

INSTITUT PASCAL
sciences de l'ingénierie et des systèmes

Real-time Harris and Stephen implementation on Smart camera

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Summary

1 - Feature Extraction,

2 - Harris & Stephen detector,

3 – The hardware implementation,

4 – The results of the implementation,

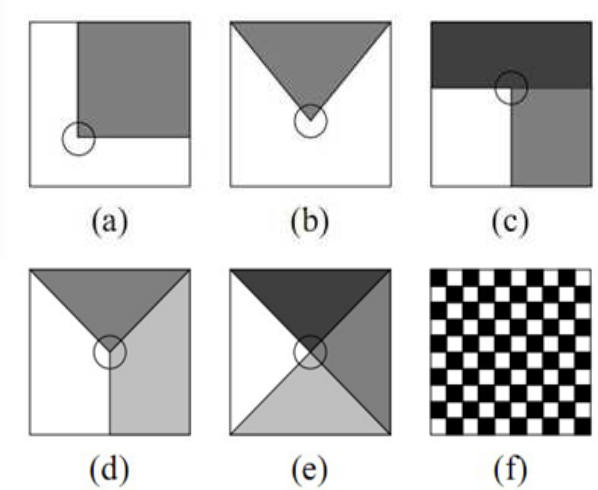
5 – The DreamCAM,

I - Feature Extraction :

is used to describe the combination of *feature detector*, and a *feature descriptor*.

Feature detector

Harris & Stephen algorithm

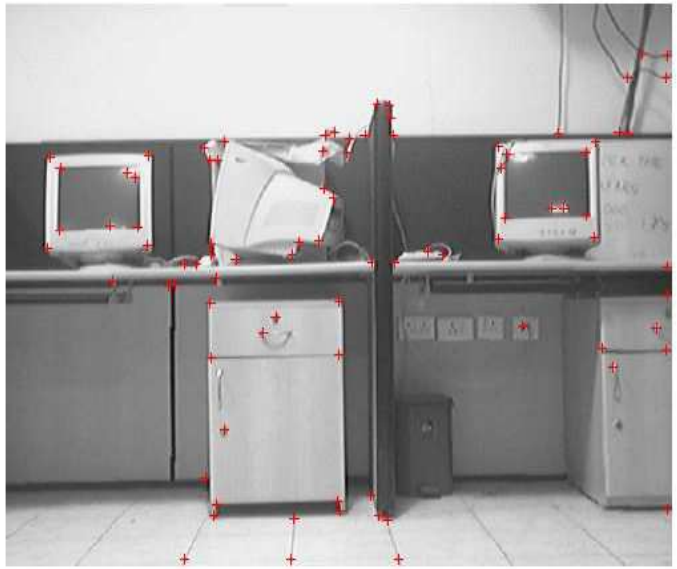


Feature descriptor

A simple descriptor, which gives for each interest point an intensity patch from the image (its neighbors).

2 - Harris & Stephen detector (1988) : 1/2

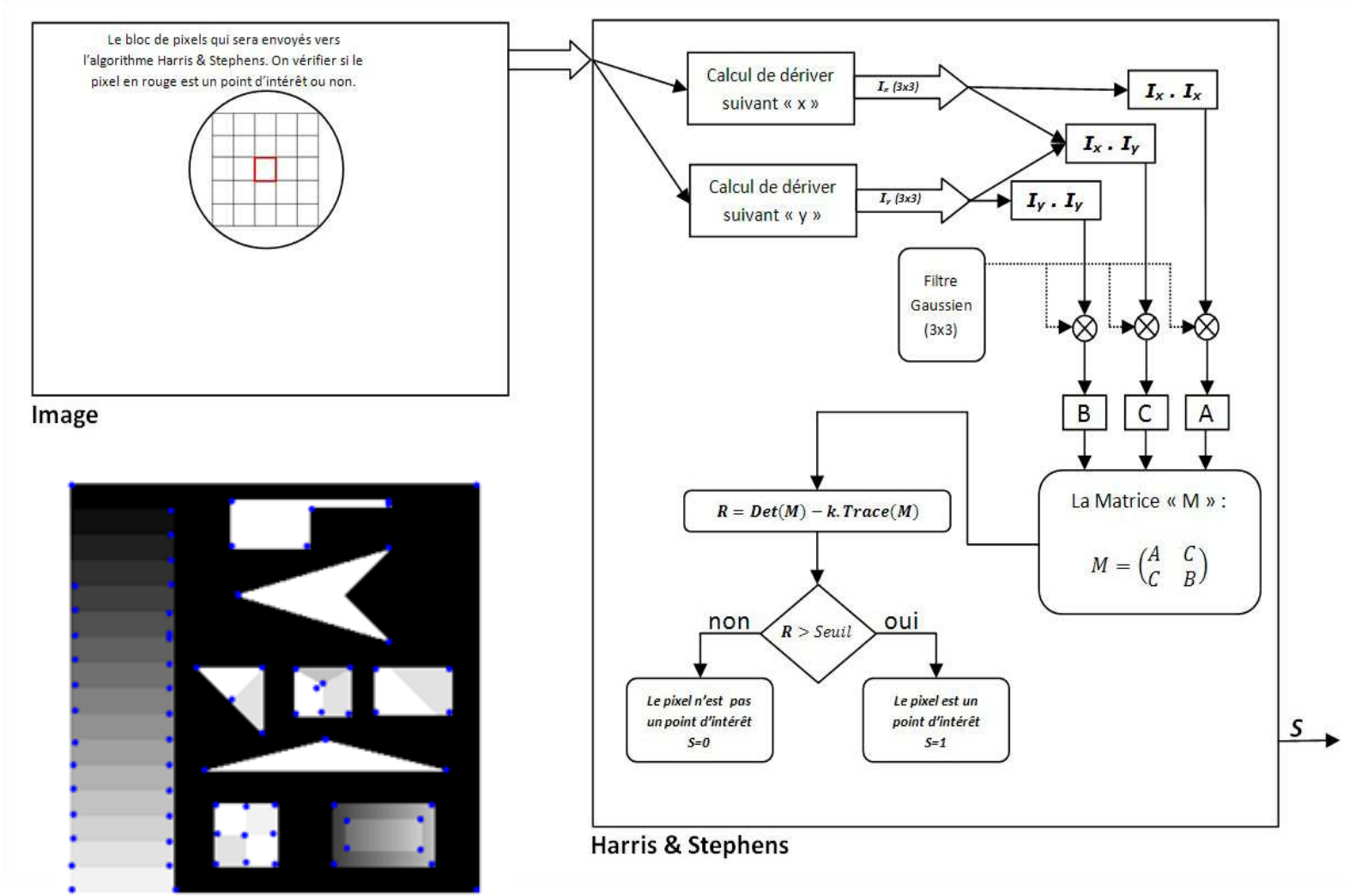
Currently, most of the computer vision algorithm use interest point of type Harris & Stephen as input.



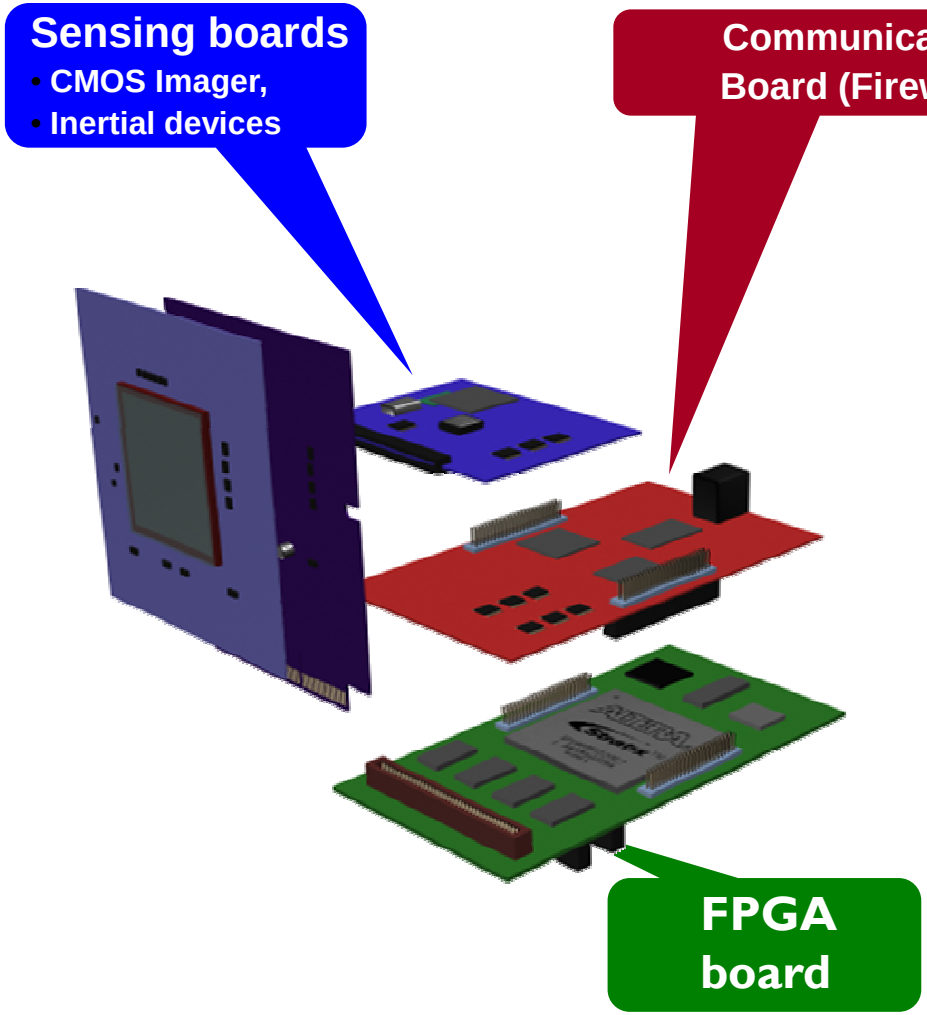
Because :

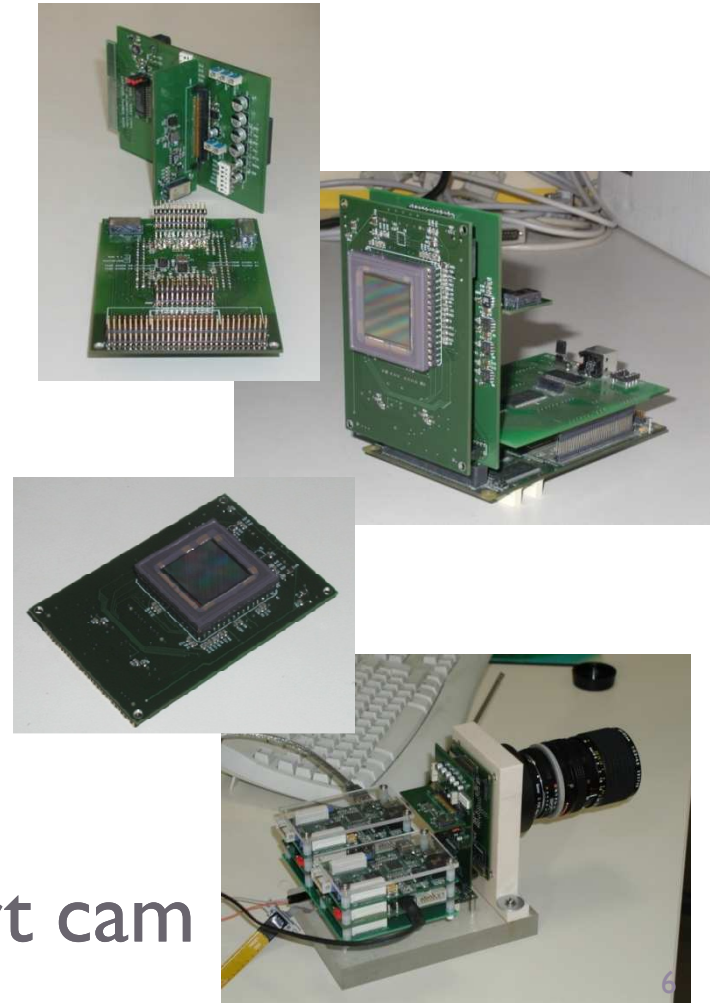
- It is based on simple principal,
- Gives acceptable results

2 - Harris & Stephen detector (1988) : 2/2



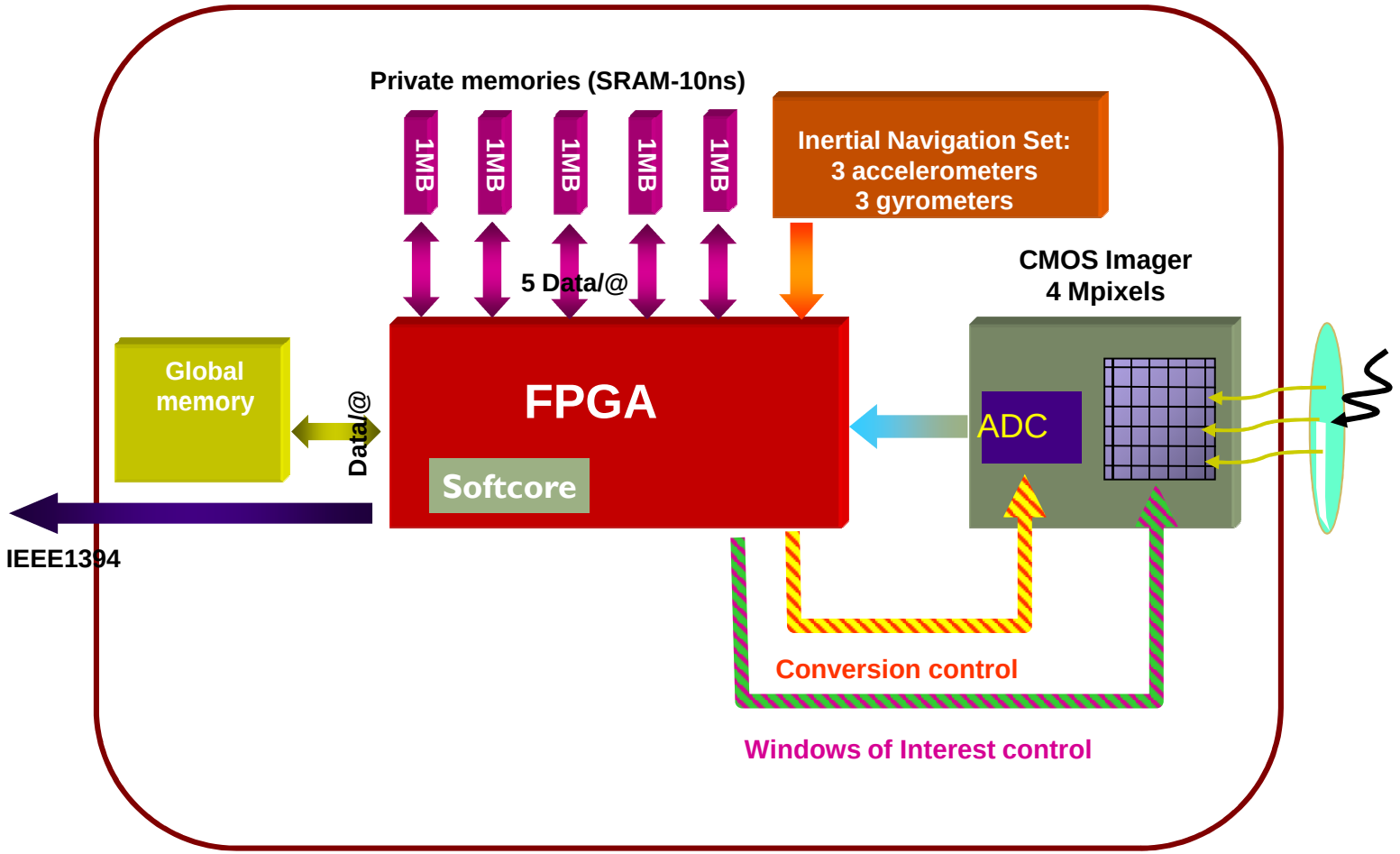
3 - The hardware implementation : 1/4





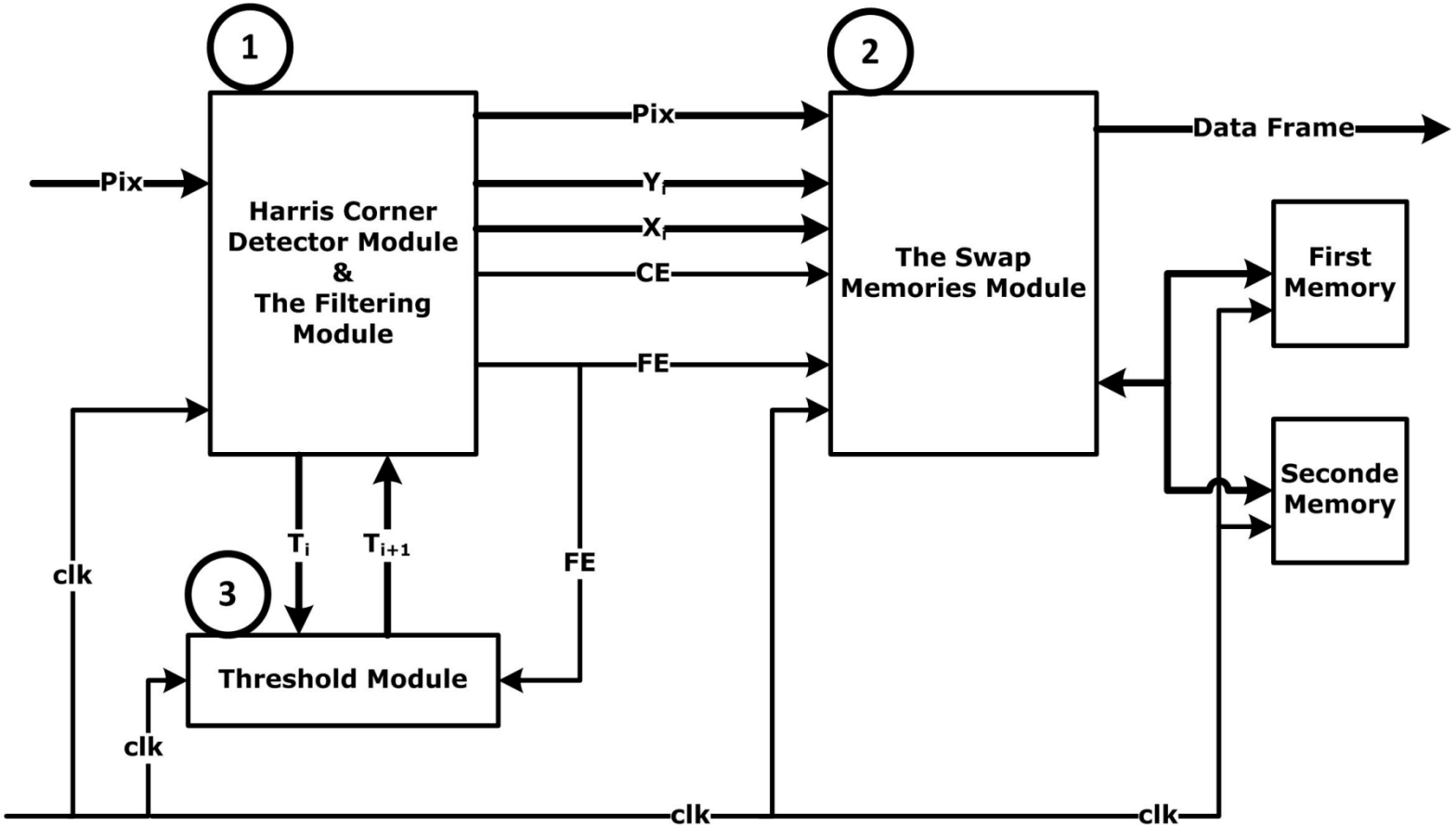
SeeMOS: FPGA-based smart cam

3 - The hardware implementation : 2/4



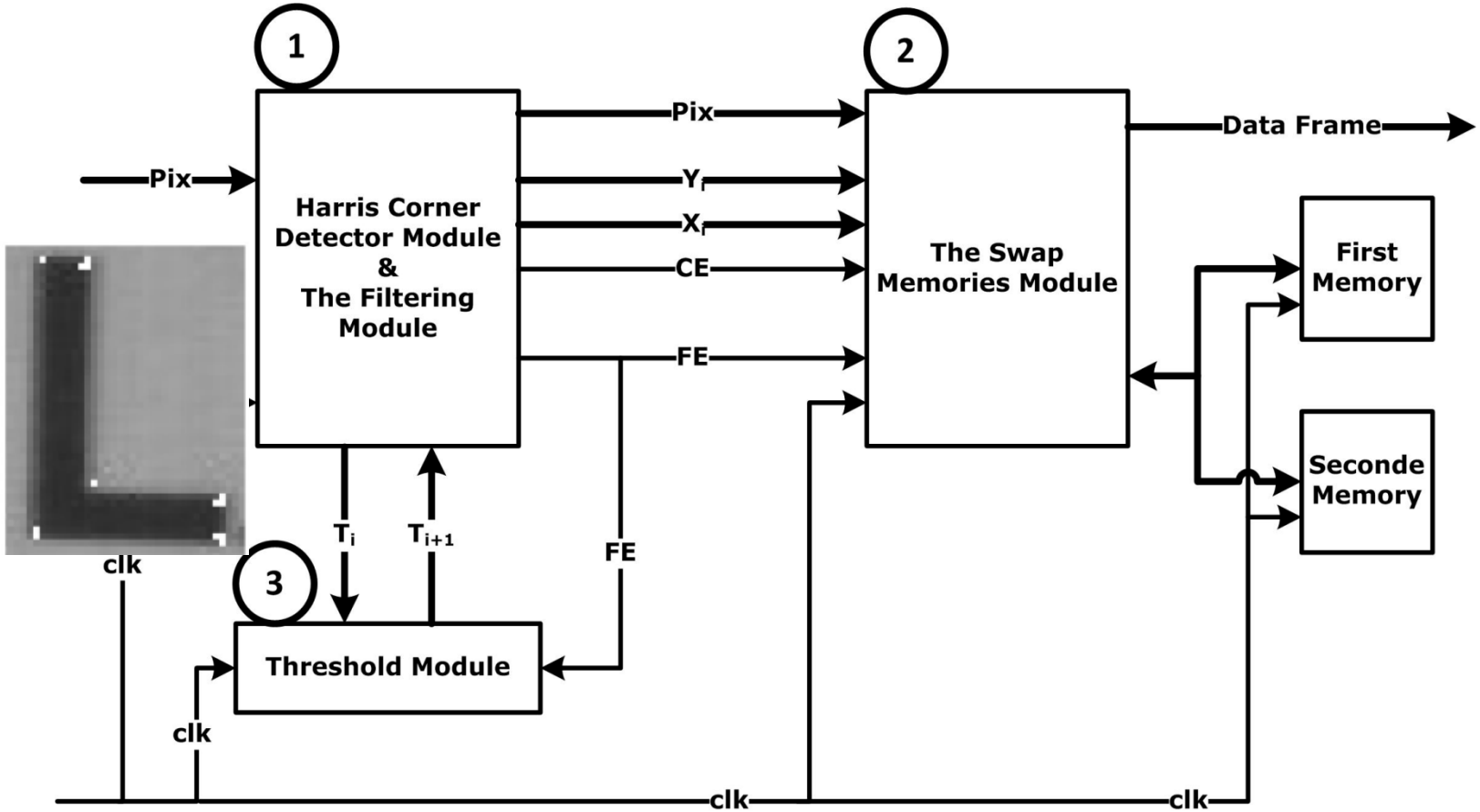
SeeMOS Synoptic

3 - The hardware implementation : 3/4



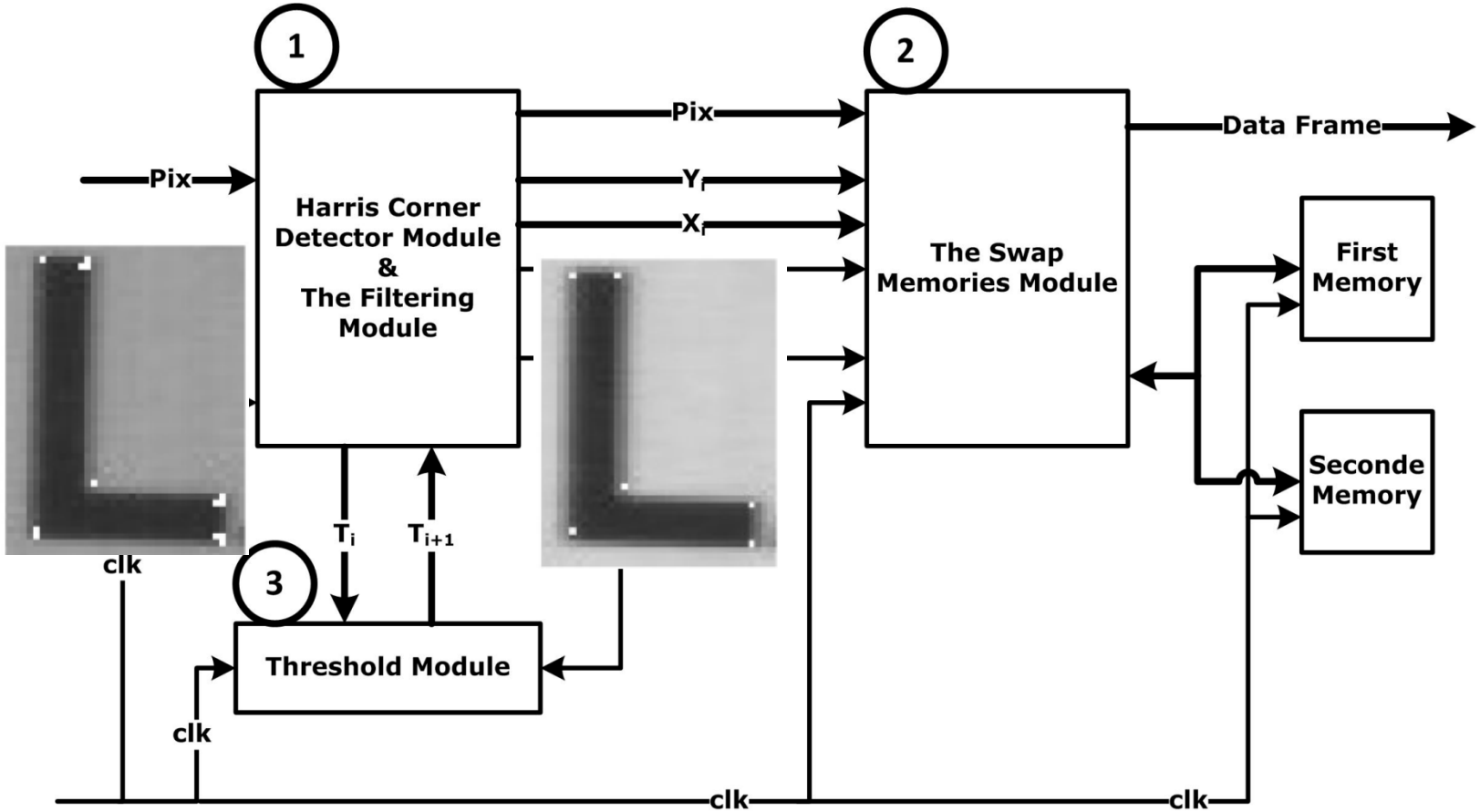
light in ⇒ data frame out

3 - The hardware implementation : 3/4



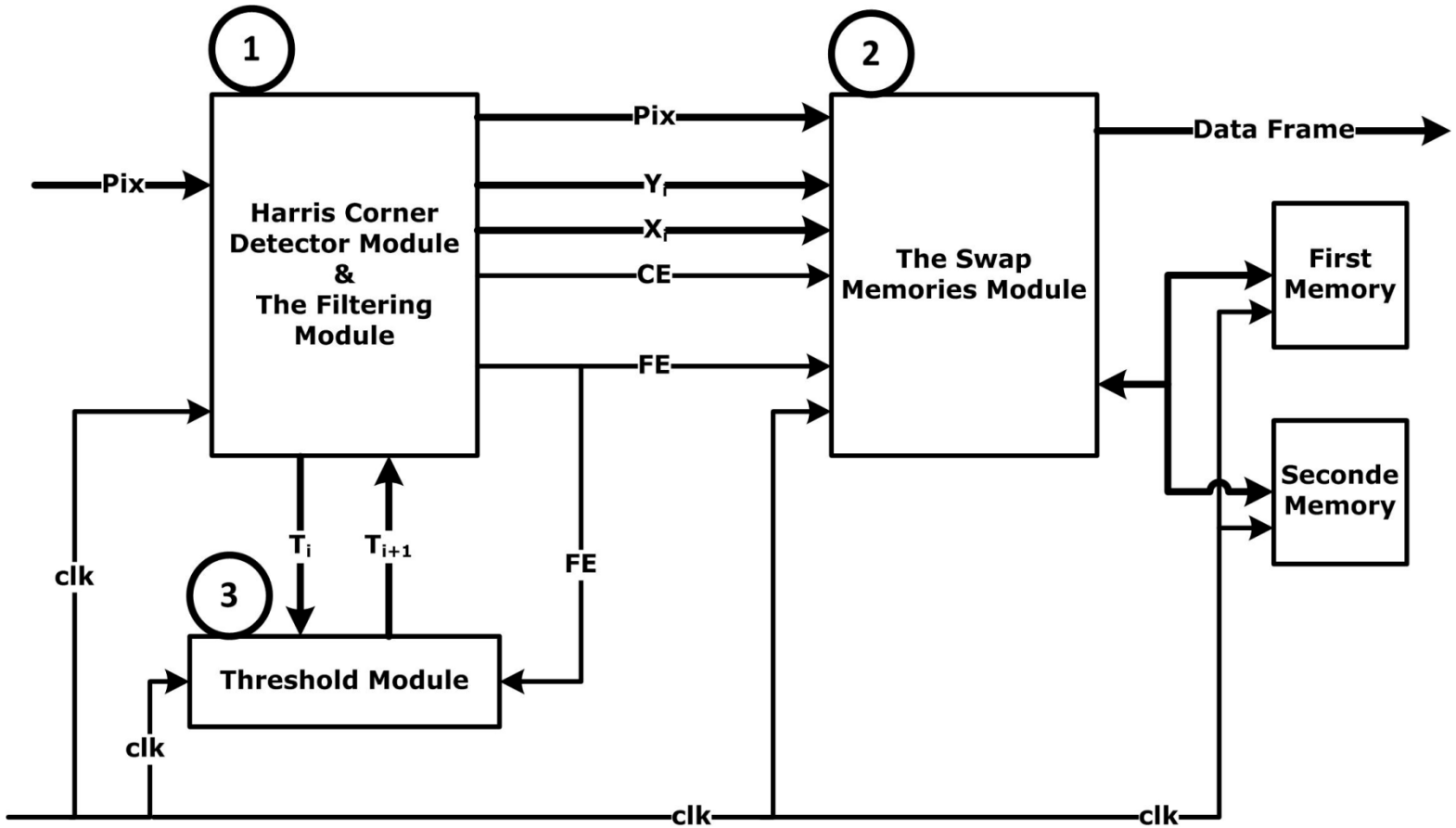
light in ⇒ data frame out

3 - The hardware implementation : 3/4



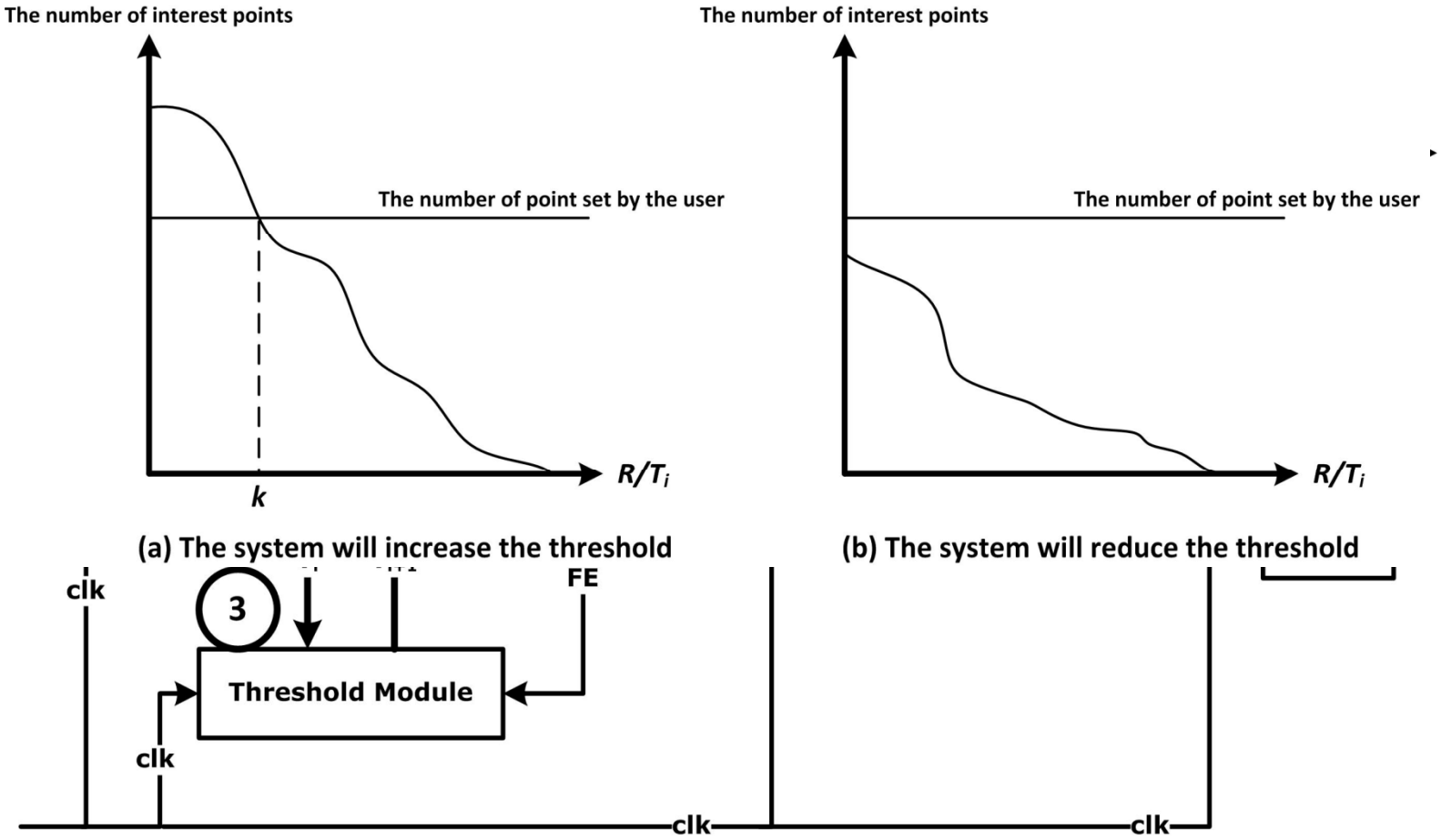
light in ⇒ data frame out

3 - The hardware implementation : 3/4



light in ⇒ data frame out

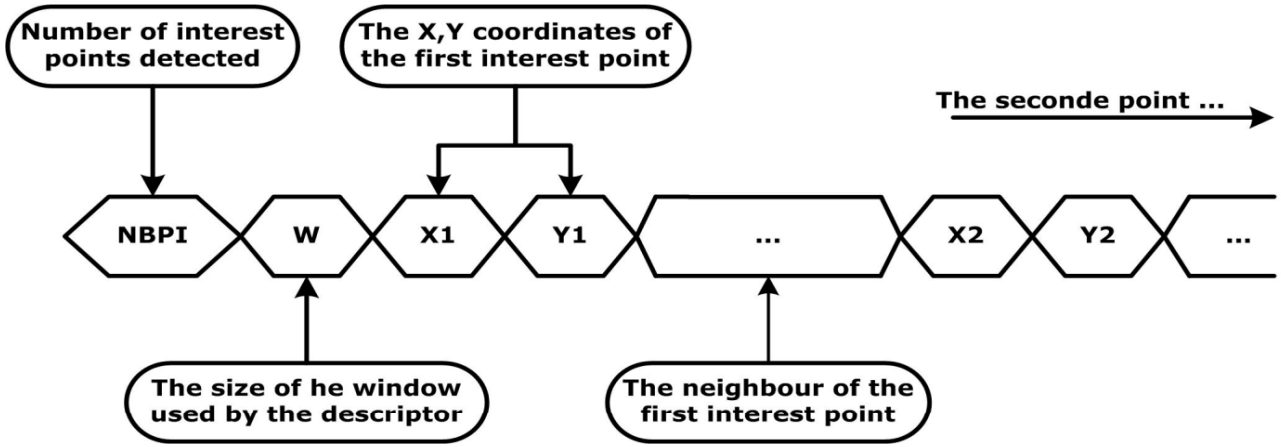
3 - The hardware implementation : 3/4

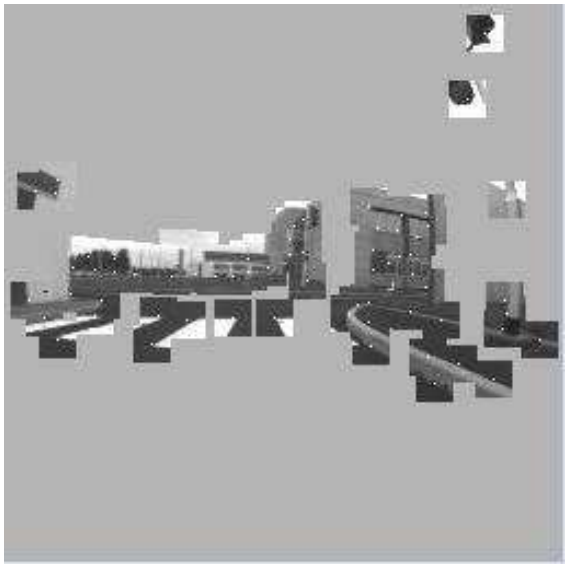


light in ⇒ data frame out

3 - The hardware implementation : 4/4

The data frame :





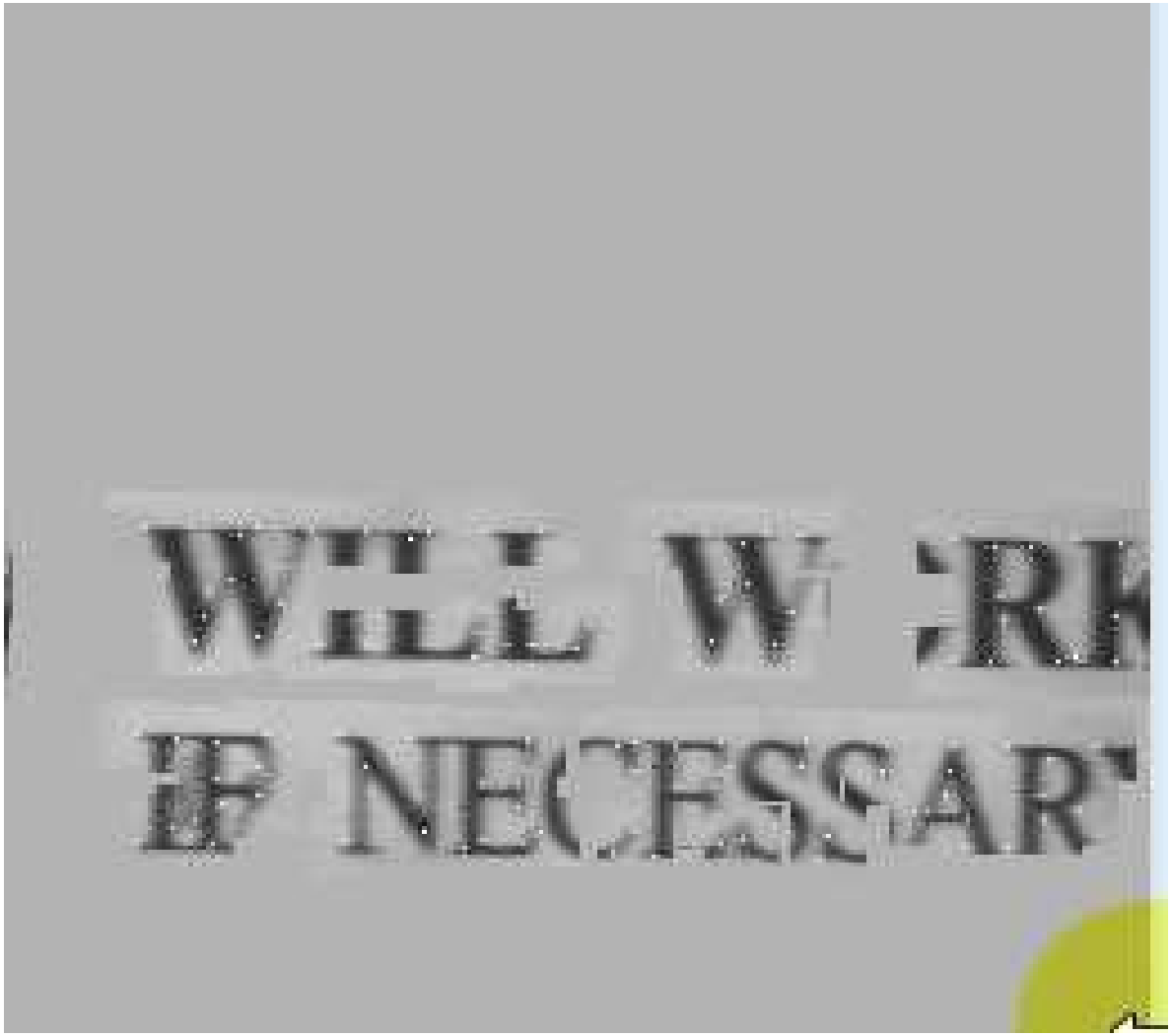
4 – The results of the implementation : 1/2

From the compilation report : (for image 256x256 pixels)

- The maximal frequency = *22.52MHz,*
- The FPGA resources used :

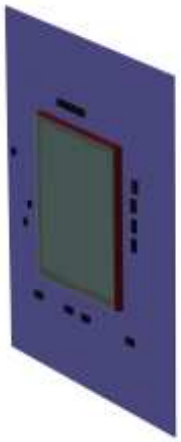
Logic Elements	**11'327 / 57'120**	**20%**
Memory Bits	**1'066'376 / 5'215'104**	**20%**
DSP-block	**33 / 44**	**23%**

4 – The results of the implementation : 2/2

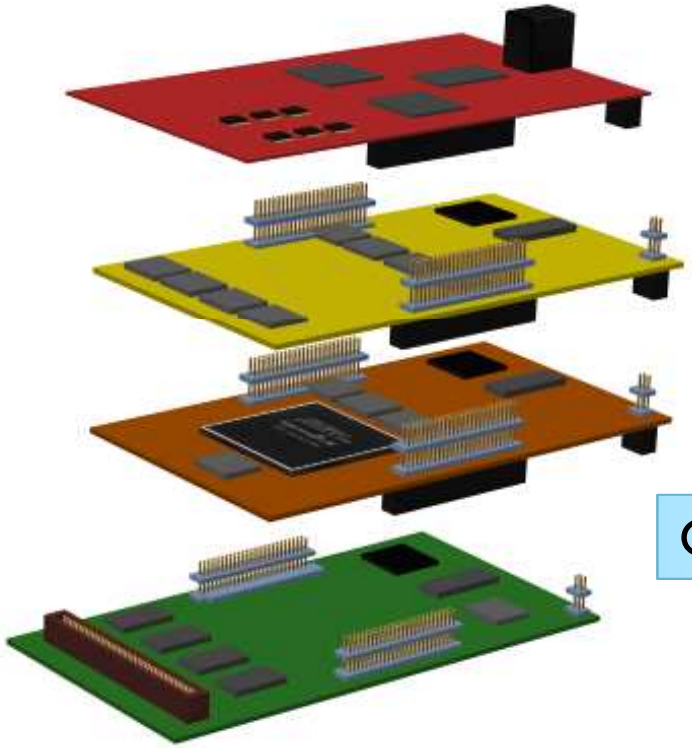


5 – The DreamCAM Anatomy :

Sensors board
(GPS, inertial,…)



IBIS5 1.3Mpixels
Image sensor



Memory board
6 x 1Mb

Cyclone III, FPGA

Power board

Thanks
For Your Attention