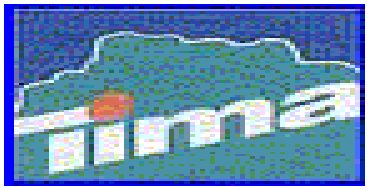
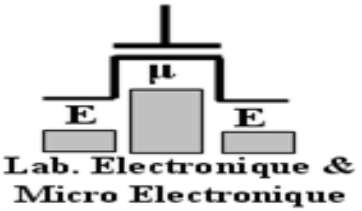




HARDWARE COMPRESSION SOLUTION BASED ON LOW COMPLEXITY ARITHMETIC ENCODING FOR LOW POWER IMAGE TRANSMISSION OVER WSNs

OUTLINE

1 Problematic

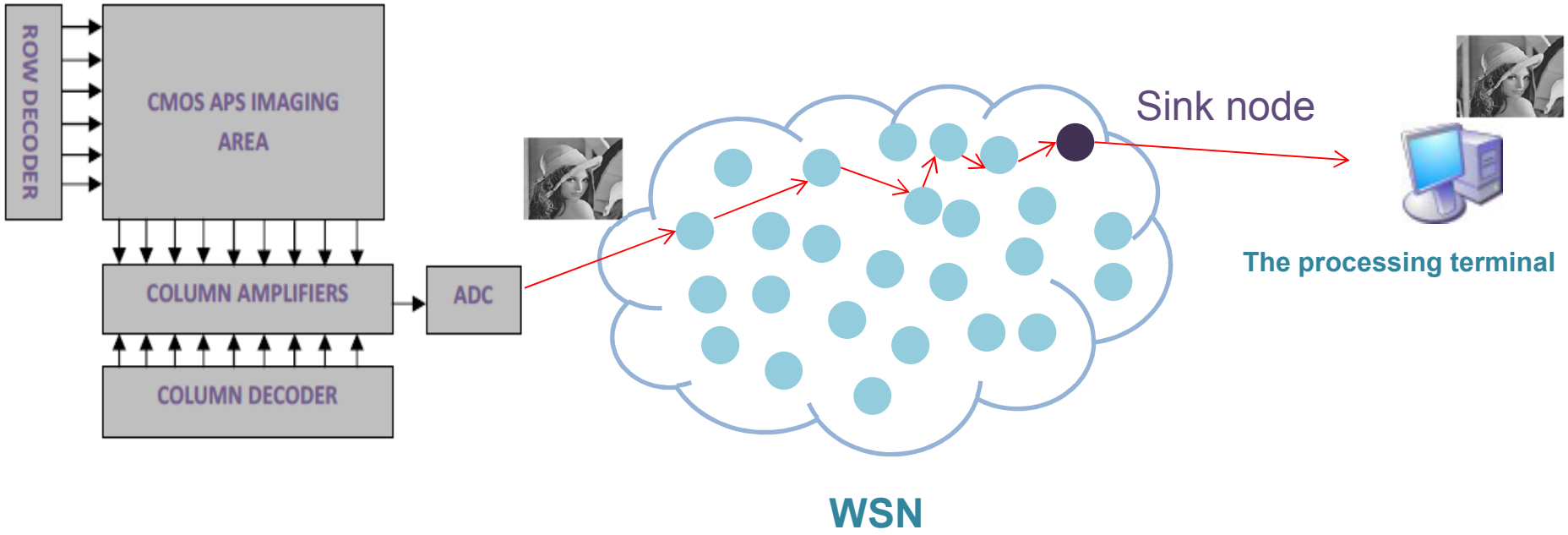
2 Compression solution for transmission over WSNs

3 Hardware implementation of the compression scheme

4 Conclusion and future work

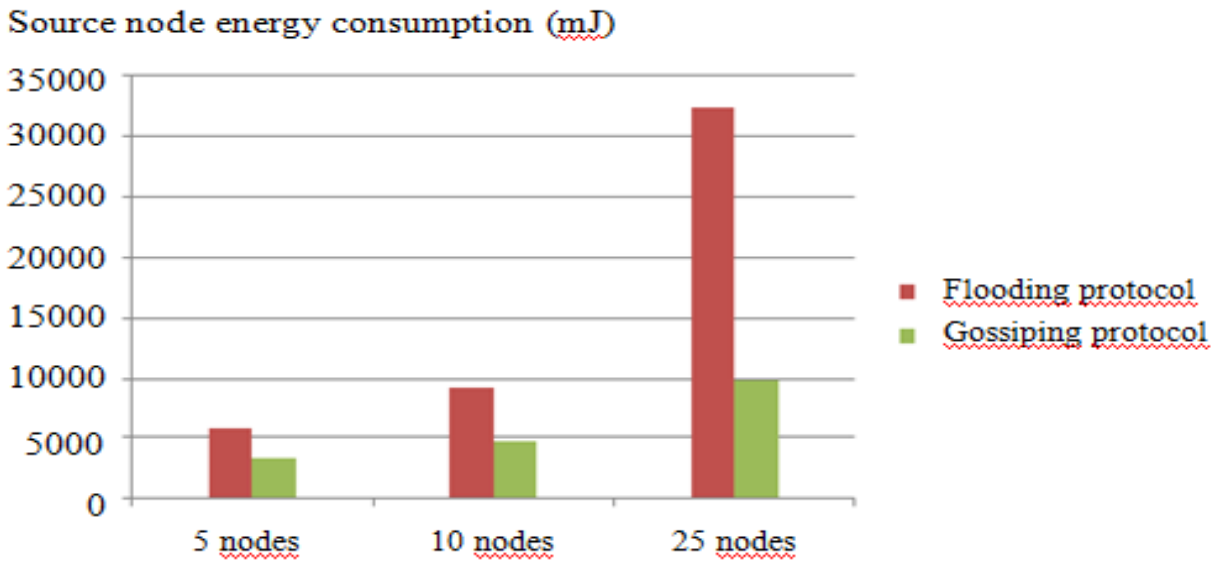
PROBLEMATIC

Transmission of uncompressed images over WSN ?



Constraints: limited lifetime, long transmission delay, …

PROBLEMATIC

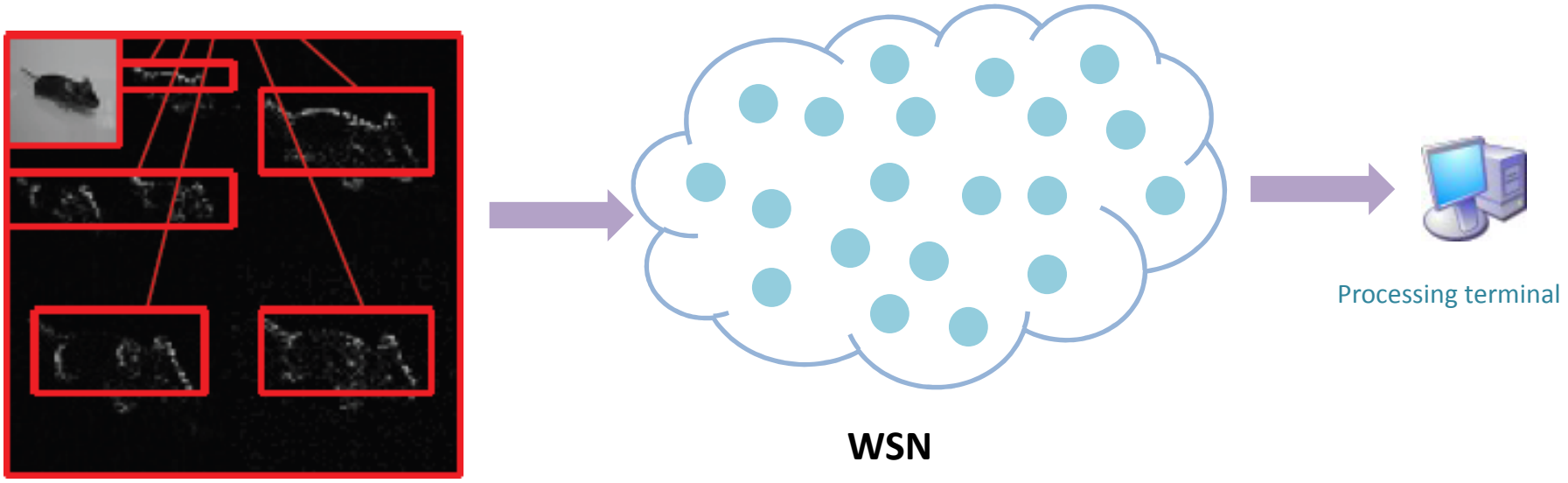


Mica2 energy consumption when transmitting a 128x128 sized image for different routing protocols.

- ✓ **Considerable energy consumption for both protocols**
- ✓ **Energy consumption increases more with the network size**

PROBLEMATIC

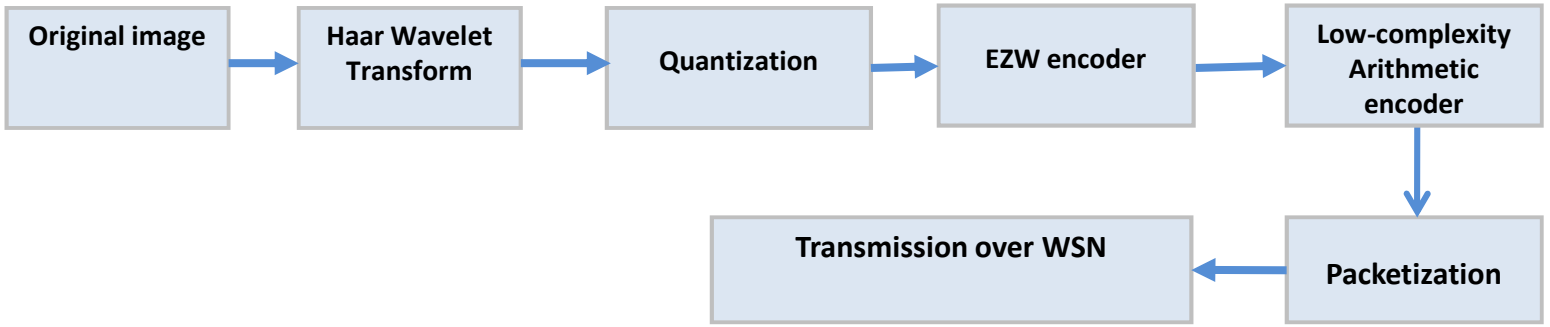
Solution : Image compression scheme for WSNs



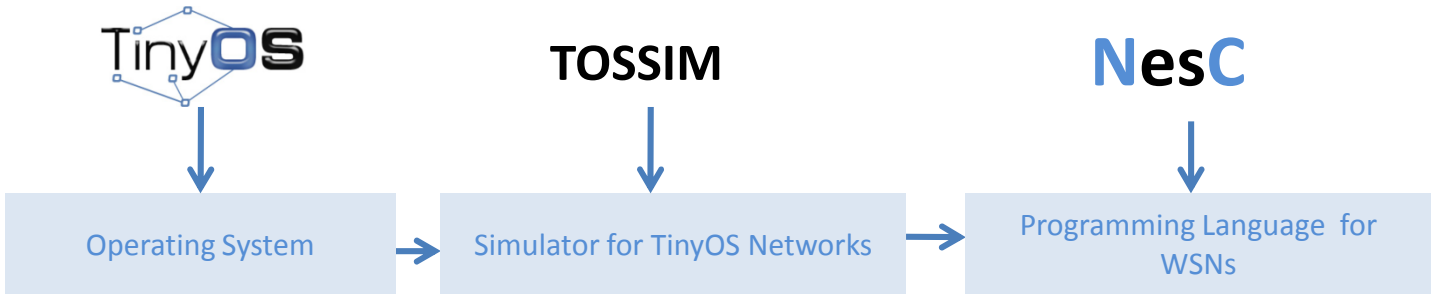
✓ Using data compression to reduce the number of bits sent reduces energy expended for transmission

✓ Increase the WSN's lifetime

COMPRESSION SOLUTION FOR TRANSMISSION OVER WSNs



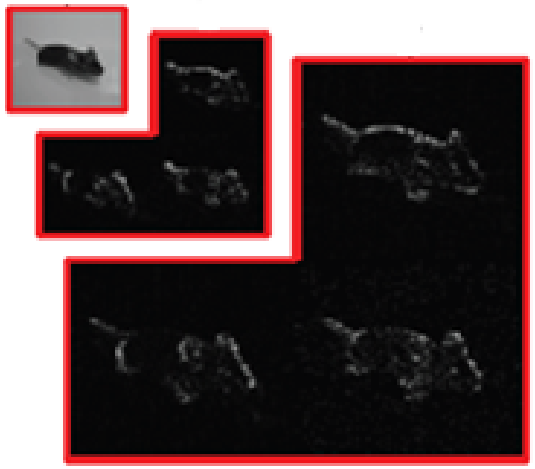
Environment



Open Source

COMPRESSION SOLUTION FOR TRANSMISSION OVER WSN

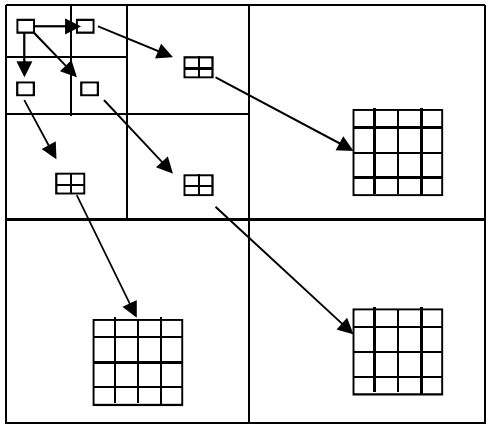
Haar Wavelet Transform

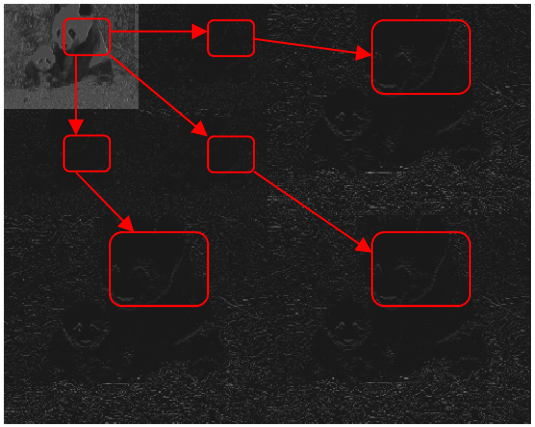


- ✓ Simplicity
- ✓ It is memory efficient
- ✓ It is exactly reversible without the edge effects
- ✓ Robust under transmission and decoding errors
- ✓ It facilitates progressive transmission of images

COMPRESSION SOLUTION FOR TRANSMISSION OVER WSN

Embedded Zerotrees of Wavelet





Dependency between the Haar Wavelet coeffecients

✓ EZW uses the dependency between the wavelet coeffecients to efficiently encode the image. It is very effective if used with HWT.

✓ EZW produces compression results that are competitive with all known compression algorithms, but with reduced complexity

Arithmetic encoding

✓ Arithmetic encoding is optimal in theory and very nearly optimal in practice : It can be proven to almost reach the best compression ratio possible.

✓ The most important advantage of arithmetic encoding is its flexibility : it can be used in conjunction with any statistical model

The main disadvantage of arithmetic coding is that it tends to be slow.

Arithmetic encoding

Standard Arithmetic encoding :

19 %

1. Compute the probabilities of occurrence for each symbol to be encoded

7 %

2. Associate to each symbol an interval proportional to its probability of occurrence.

74 %

3. Start coding the data sequence

COMPRESSION SOLUTION FOR TRANSMISSION OVER WSN

Arithmetic encoding

Low-complexity Arithmetic encoding :

19 %

1. ~~Compute the probabilities of occurrence for each symbol to be encoded~~

7 %

2. Associate to each symbol an interval proportional to its probability of occurrence.

74 %

3. Start coding the data sequence

Arithmetic encoding

Low-complexity Arithmetic encoding :

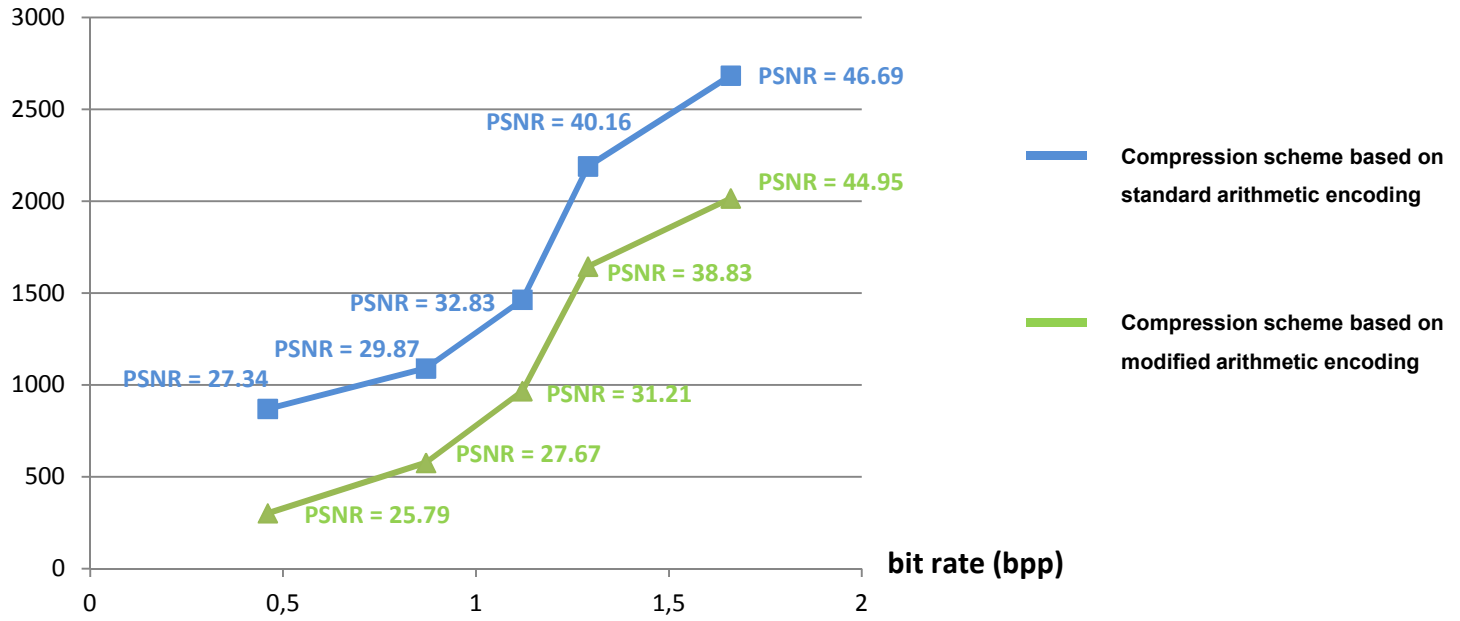
1. Use a predefined statistical model, which is extracted using a reference image with the same characteristics (size, depth, …).

2. Associate to each symbol an interval proportional to its probability of occurrence.

3. Start coding the data sequence

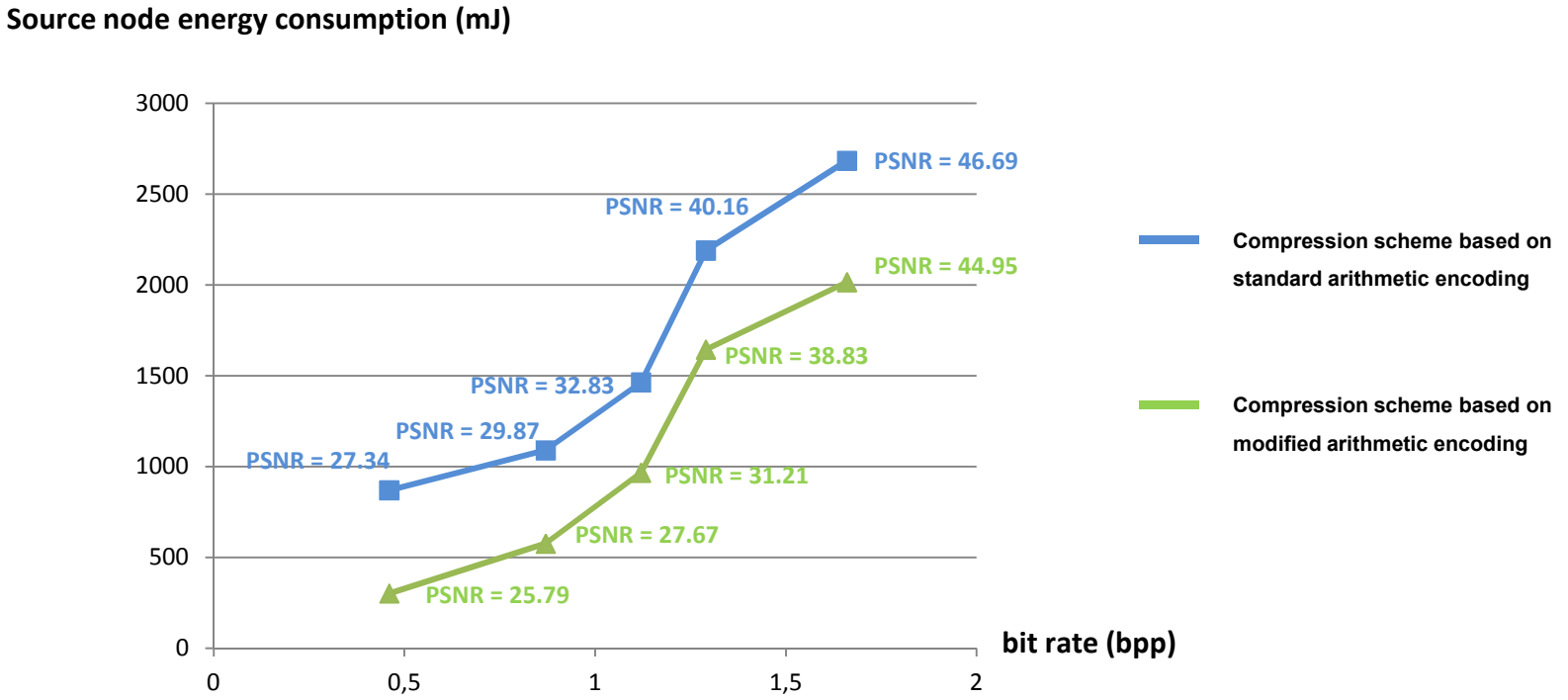
COMPRESSION SOLUTION FOR TRANSMISSION OVER WSN

Source node energy consumption (mJ)



Mica2 energy consumption when transmitting a compressed image of size 128x128 8-bpp

COMPRESSION SOLUTION FOR TRANSMISSION OVER WSN

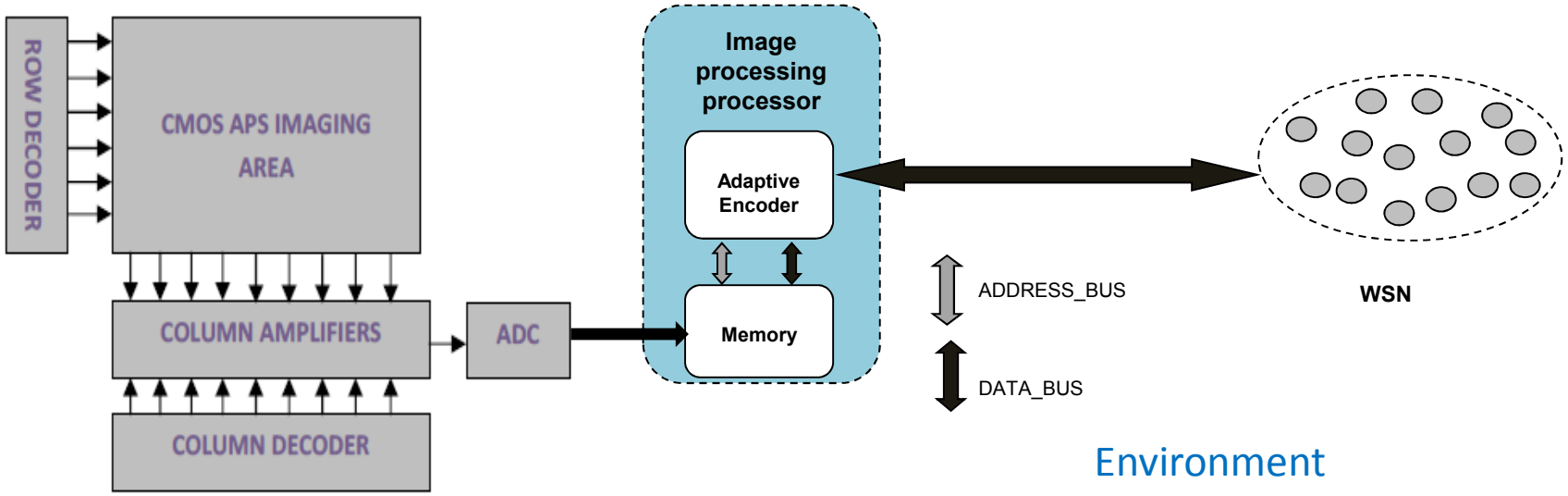


Mica2 energy consumption when transmitting a compressed image of size 128x128 8-bpp

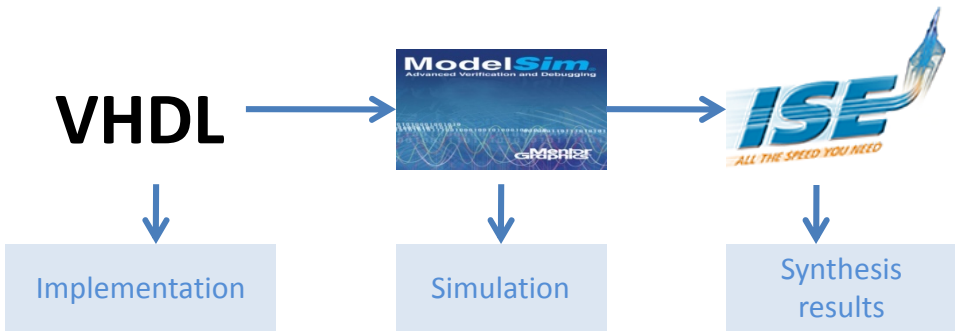
Necessity of a hardware implementation to reduce required power while maintaining good reconstructed image quality

HARDWARE IMPLEMENTATION OF THE COMPRESSION SCHEME

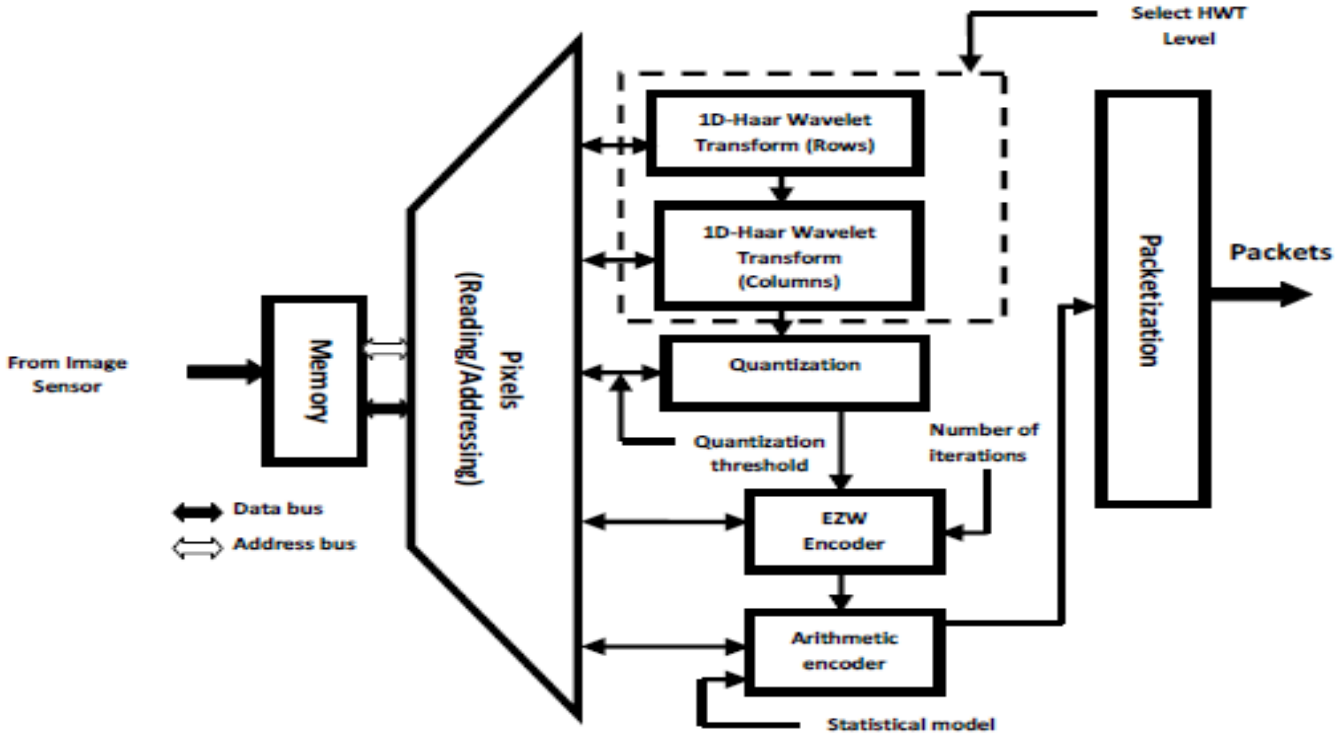
Hardware solution



Environment



HARDWARE IMPLEMENTATION OF THE COMPRESSION SCHEME



Block diagram of the image compression circuit

- ✓ The circuit reduces the required power and the processing time for image compression
- ✓ The circuit will be acting as image encoder co-processor for the source node microcontroller

HARDWARE IMPLEMENTATION OF THE COMPRESSION SCHEME

The encoder performances for FPGA circuit

	Frequency (MHz)	Estimated processing time (ms)	Dynamic power (mW)	Estimated energy (mJ)
The compression circuit	113.84	17.84	270	4.81

HARDWARE IMPLEMENTATION OF THE COMPRESSION SCHEME

The encoder performances for FPGA circuit

	Frequency (MHz)	Estimated processing time (ms)	Dynamic power (mW)	Estimated energy (mJ)
The compression circuit	113.84	17.84	270	4.81

With regard to software TinyOS results, the FPGA solution saves more than 98 % the required energy.

HARDWARE IMPLEMENTATION OF THE COMPRESSION SCHEME

Synthesis results for the different circuit blocks and for the whole encoder architecture

	Logic cells	Frequency (MHz)
HWT + quantization	769	248.60
EZW	1253	171.15
Arithmetic encoding	149	188.63
Packetizer	87	311.27
Encoder circuit	2258	113.84

EZW and Arithmetic encoding blocks have the lowest processing frequency within the four main blocks. Given that, the frequency of the global encoder circuit will be slowed by these modules.

HARDWARE IMPLEMENTATION OF THE COMPRESSION SCHEME

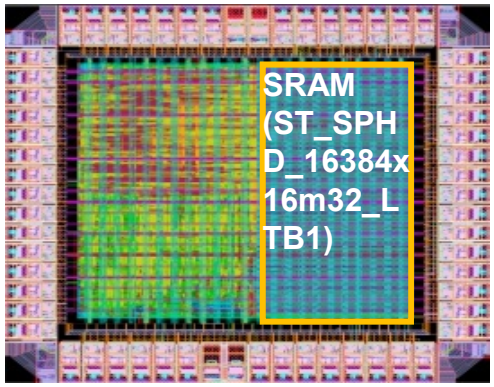
Synthesis for ASIC circuit

		Fmax (MHz)	Dynamic power (mW)	Cell area (mm2)
The compression circuit	45 nm	790	20.76	0.065
	90 nm	392	23.17	0.17
	0.13 µm	347	31.87	0.22
	0.18 µm	215	44.13	0.59
	0.35 µm	139	57.60	2.31
	0.6 µm	78	75.74	11.27

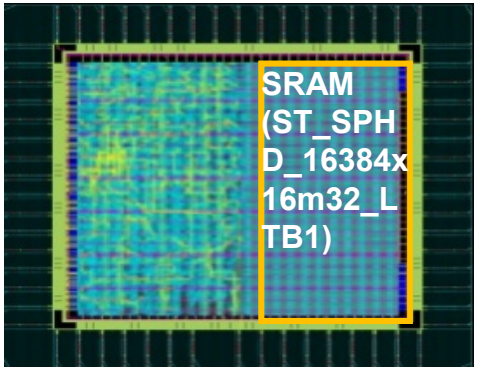
- ✓ Low power consumption and high operating frequency
- ✓ The ASIC circuit is six times faster than the FPGA solution

HARDWARE IMPLEMENTATION OF THE COMPRESSION SCHEME

Layout of the proposed encoder chip



Placement and routing of compression chip



Clock tree routing

CONCLUSION AND FUTURE WORK

- ✓ **The hardware solution looks to be very attractive for image compression in WSNs**
- ✓ **The solution is intended to be embedded as a coprocessor to the source node**
- ✓ **As a future work, we are currently improving our encoder, in order to control both the spatial and temporal redundancy, instead of removing only the spatial redundancy**

THANK YOU