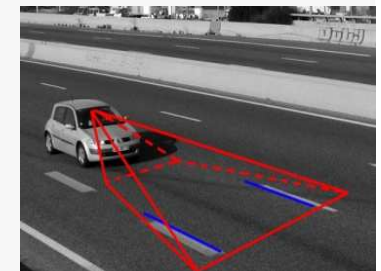


FAST PROTOTYPING OF EMBEDDED IMAGE PROCESSING APPLICATION ON HOMOGENOUS SYSTEM



A Model-driven approach for real-time road recognition on Homogeneous Network of Communicating Processors (HNCP)

Hanen Chenini, Loïc Sieler, Mohamed Amine Boussadi, Thierry Tixier, Jean-Pierre Dérutin,
Alexis Landrault and Romuald Aufrère



Outline

1. Context
2. Real time parallel implementation on SoPC
(System on Programmable Chip)
3. Model-driven approach for real-time road
recognition
4. Experiments && Conclusion



Context



General Context

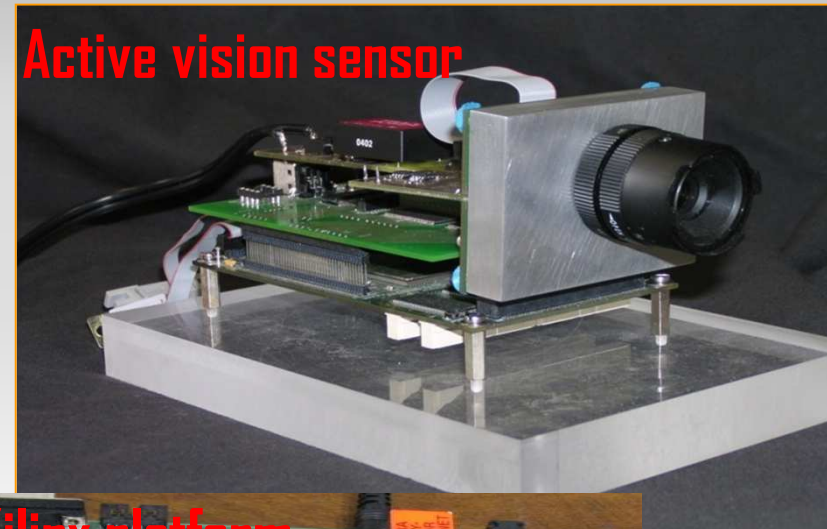
1. Context

embedded vision system

Embedded Vision System

- CMOS imager
- Embedded treatment
- SoC approach

Active vision sensor



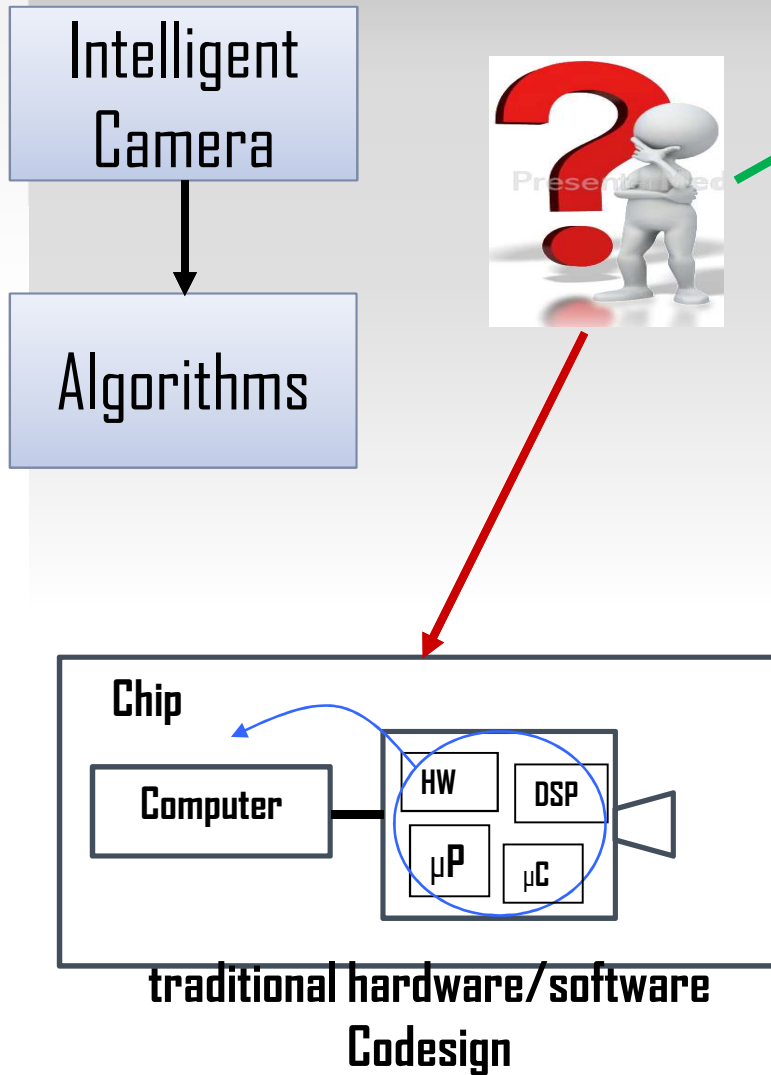
SoPC Xilinx platform



**PROBLEMATIC :
INCREASING COMPLEXITY
OF THE CONCEPTION OF SOC**

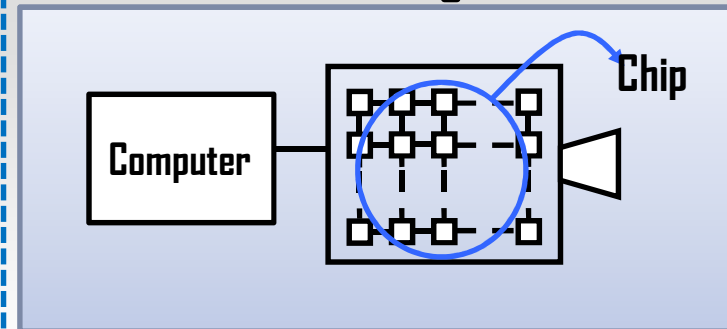


SoC design challenges



LASMEA's Approach

Rapid prototyping process
of Parallel algorithms



Fast Prototyping of Embedded
Image Processing on
Homogeneous Network of
Communicating Processor
(HNCP)



Real time parallel implementation on System on Programmable Chip



The HNCP Methodology

- Homogeneous Network of Communicating Processors on SoPC.

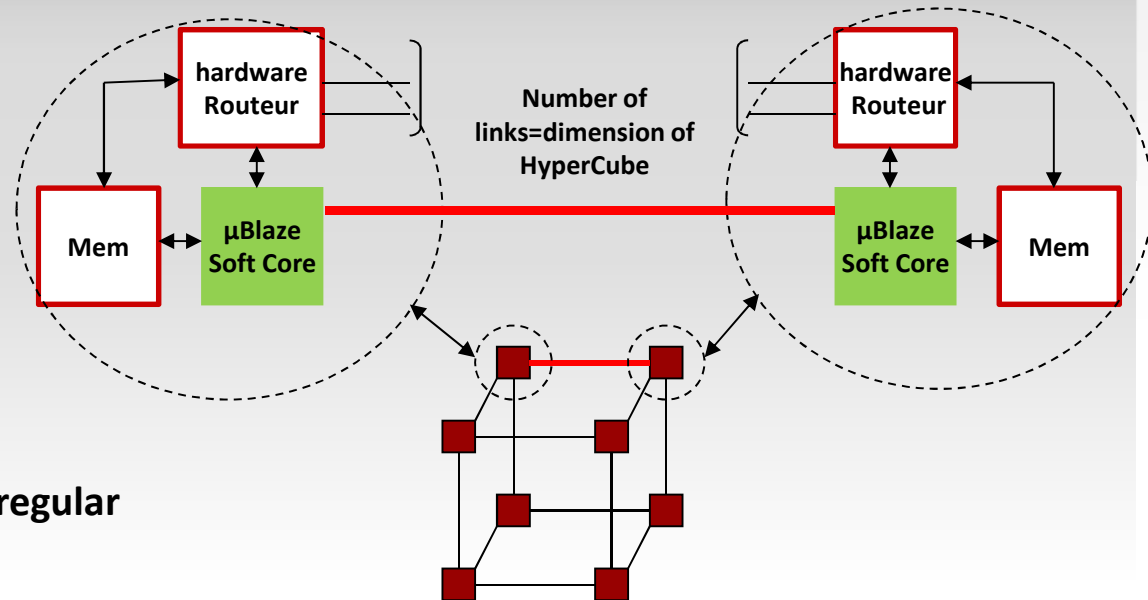
- The generic architecture model chosen is the type MIMDDM.

- The static topology choice is the hypercube.

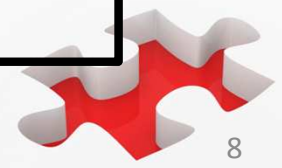
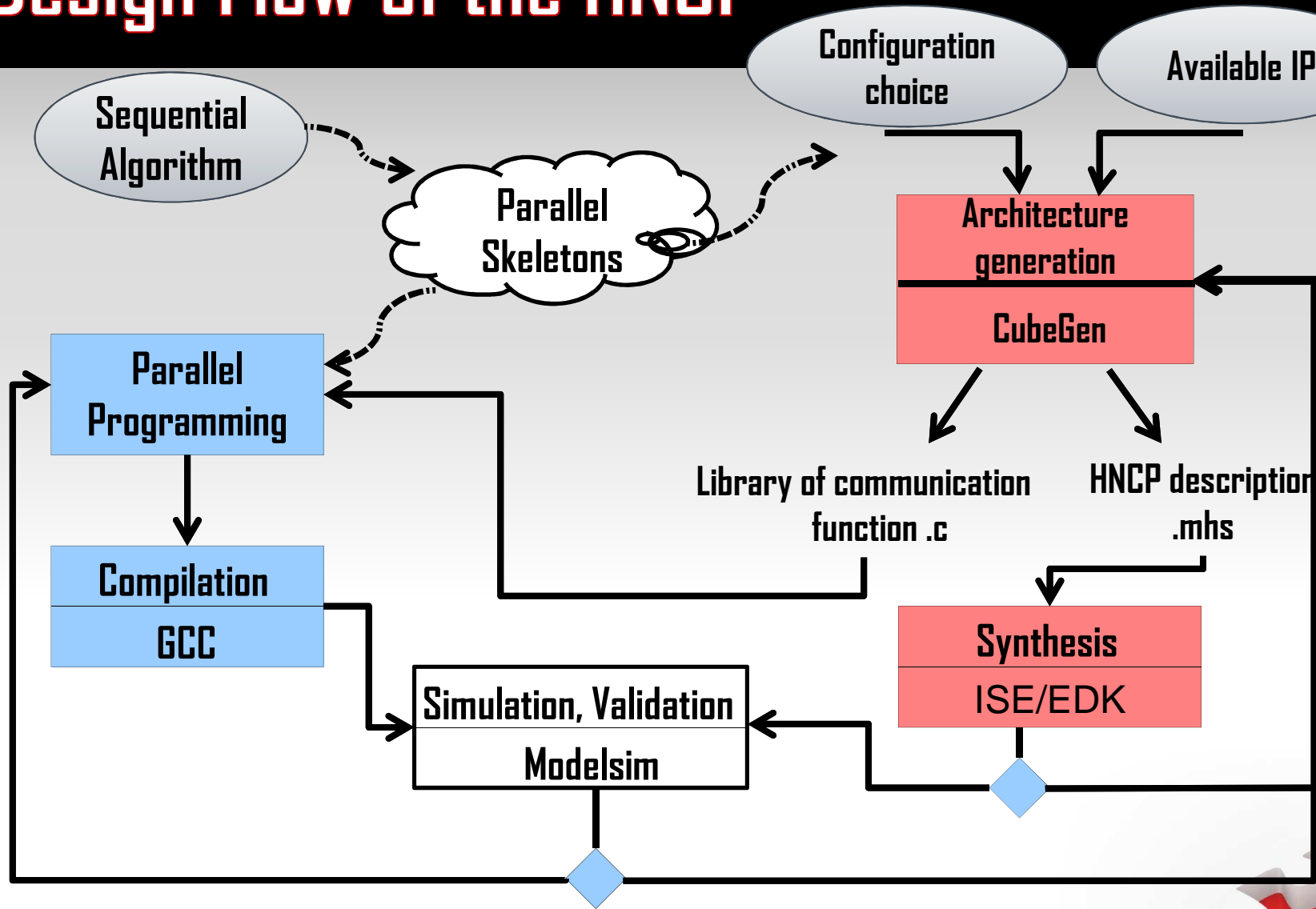
- This parametrizable architecture is regular and homogeneous.

- Direct point to point links and the other using a hardware router.

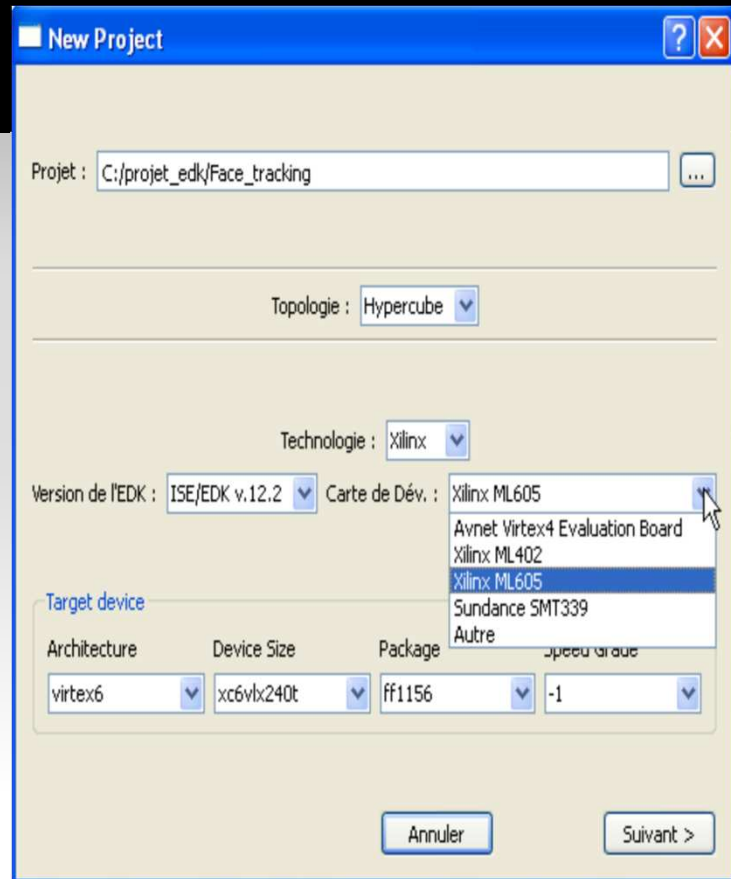
- Parametrization of the HNCP via the CubeGen Framework (dimension, communication ,Size of memory, Configurations of softcore...).



Design Flow of the HNCP



CubeGen Interface



New Project

Projet : C:/projet_edk/Face_tracking

Topologie : Hypercube

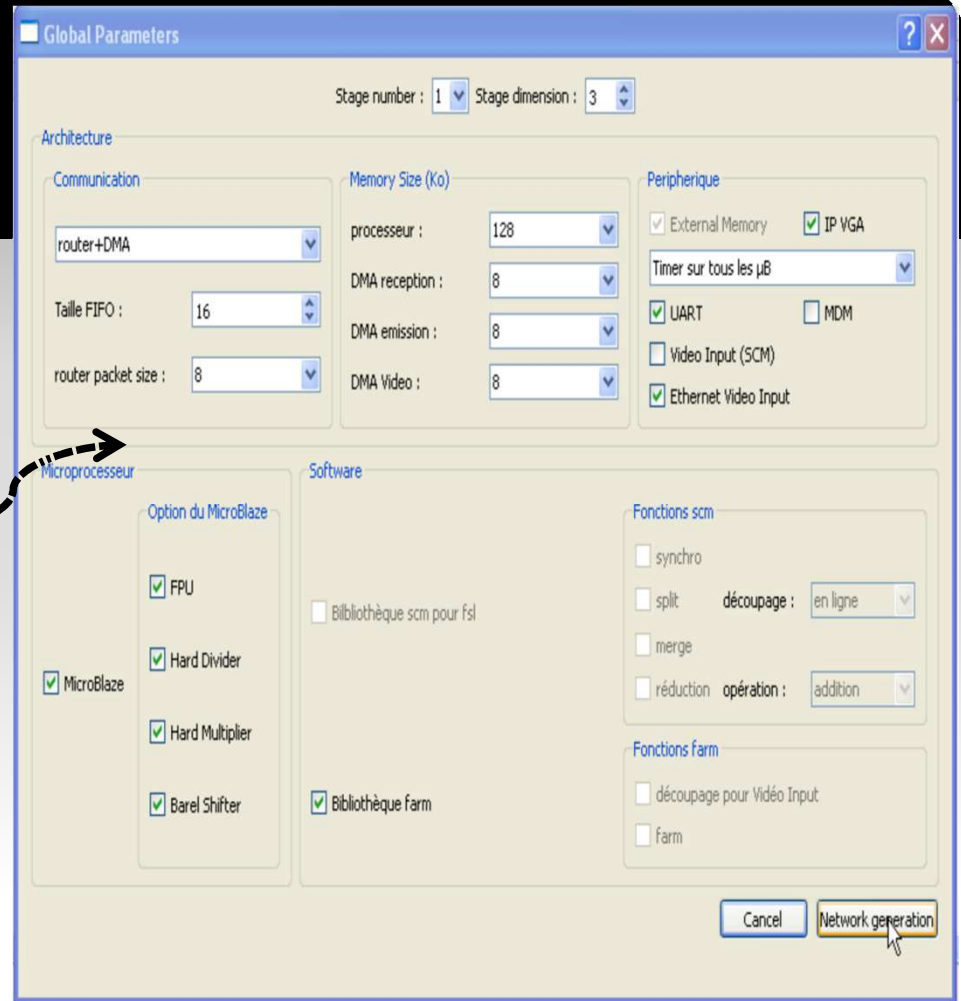
Technologie : Xilinx

Version de l'EDK : ISE/EDK v.12.2 Carte de Dév. : Xilinx ML605

Target device

Architecture	Device Size	Package	Speed Grade
virtex6	xc6vlx240t	ff1156	-1

Buttons: Annuler, Suivant >



Global Parameters

Stage number : 1 Stage dimension : 3

Architecture

Communication: router+DMA

Memory Size (Ko): processeur : 128, DMA reception : 8, DMA emission : 8, DMA Video : 8

Peripherique: External Memory, IP VGA, Timer sur tous les µB, UART, MDM, Video Input (SCM), Ethernet Video Input

Microprocesseur

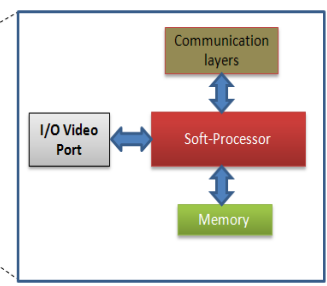
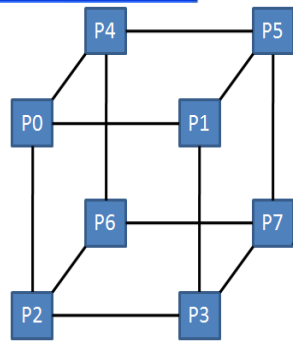
Option du MicroBlaze: FPU, Hard Divider, Hard Multiplier, Barrel Shifter, MicroBlaze

Software: Bibliothèque scm pour fsl, Bibliothèque farm

Fonctions scm: synchro, split découpage : en ligne, merge, réduction opération : addition

Fonctions farm: découpage pour Vidéo Input, farm

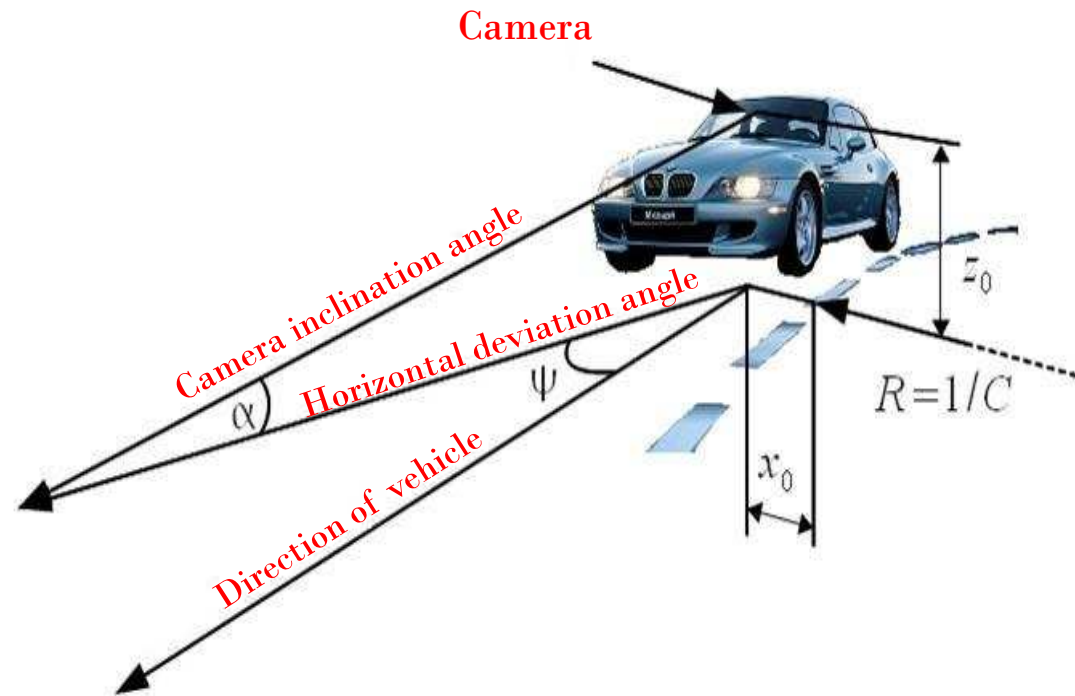
Buttons: Cancel, Network generation



Model-driven approach
for real-time road recognition



road recognition approach



The steps contained in our proposed recognition process are :

- Learning phase
- Recognition phase.



road recognition approach

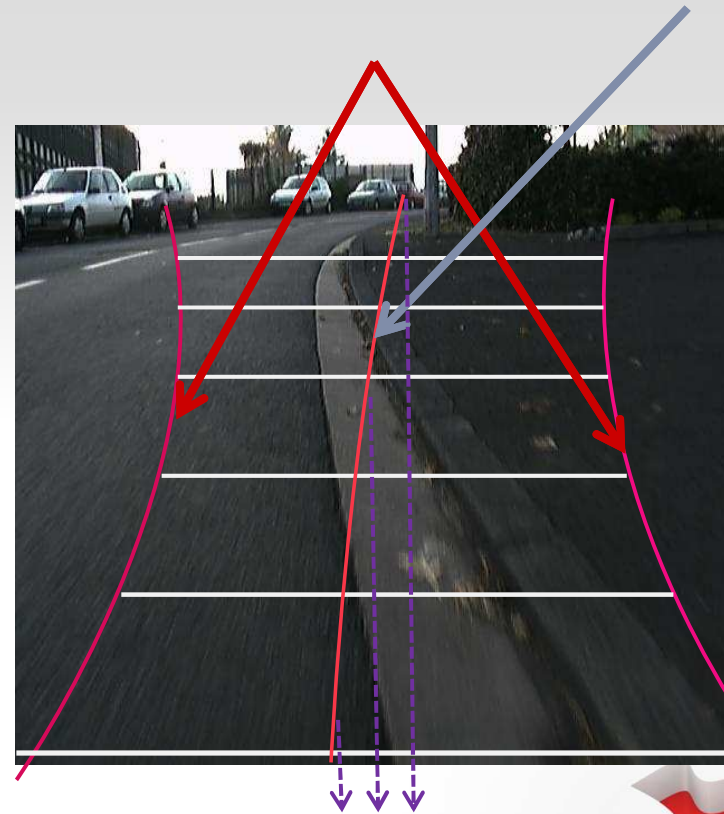
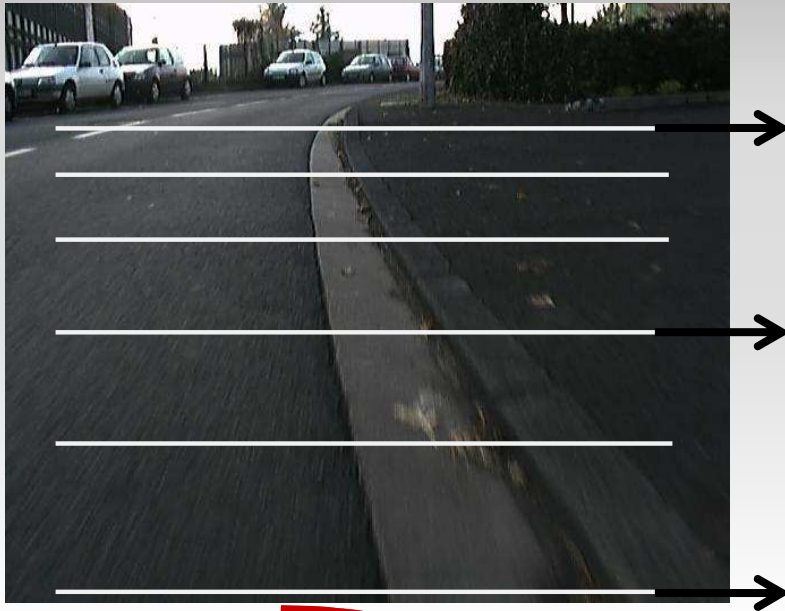
This method is based on recursive recognition driven by a probabilistic model of the road edges in the image.

- The model used is based on image data and camera parameters.
- Our statistical model is composed of n image parameters.
- This model is represented by a vector and its covariance matrix :

$$X_d = \begin{pmatrix} u_{1l} \\ \cdot \\ \cdot \\ \cdot \\ u_{nl} \end{pmatrix} \text{ and } C_{X_d} = \begin{pmatrix} \sigma_{1l}^2 & \cdot & \cdot \\ \vdots & \ddots & \cdot \\ \cdot & \cdot & \sigma_{1n}^2 \end{pmatrix}$$



Learning step

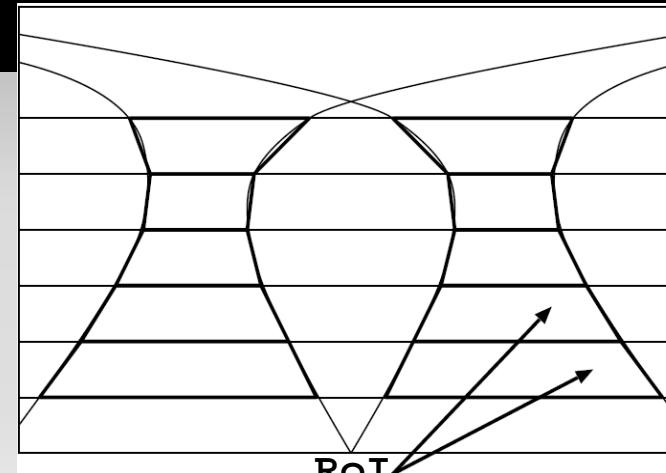
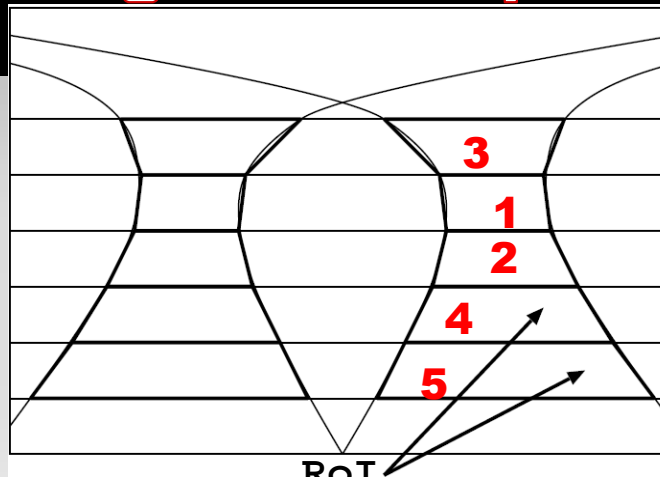


$$X_d = \begin{pmatrix} u_{1l} \\ \cdot \\ \cdot \\ \cdot \\ u_{nl} \end{pmatrix} = g(V_i, X_0, \omega, \alpha, C, L)$$



3. Model-driven approach for real-time road recognition

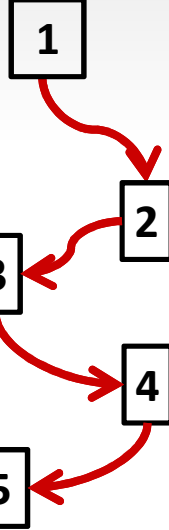
Recognition step



Regions of Interest

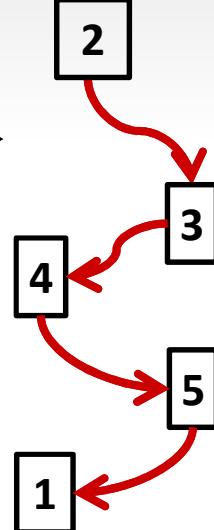
Regions of Interest

Hypothesis 1



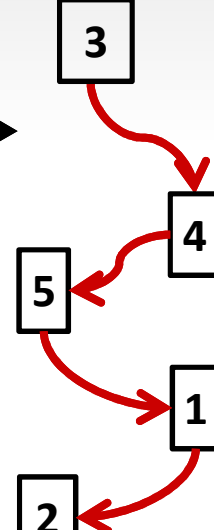
Score of recognition 1

Hypothesis 2



Score of recognition 2

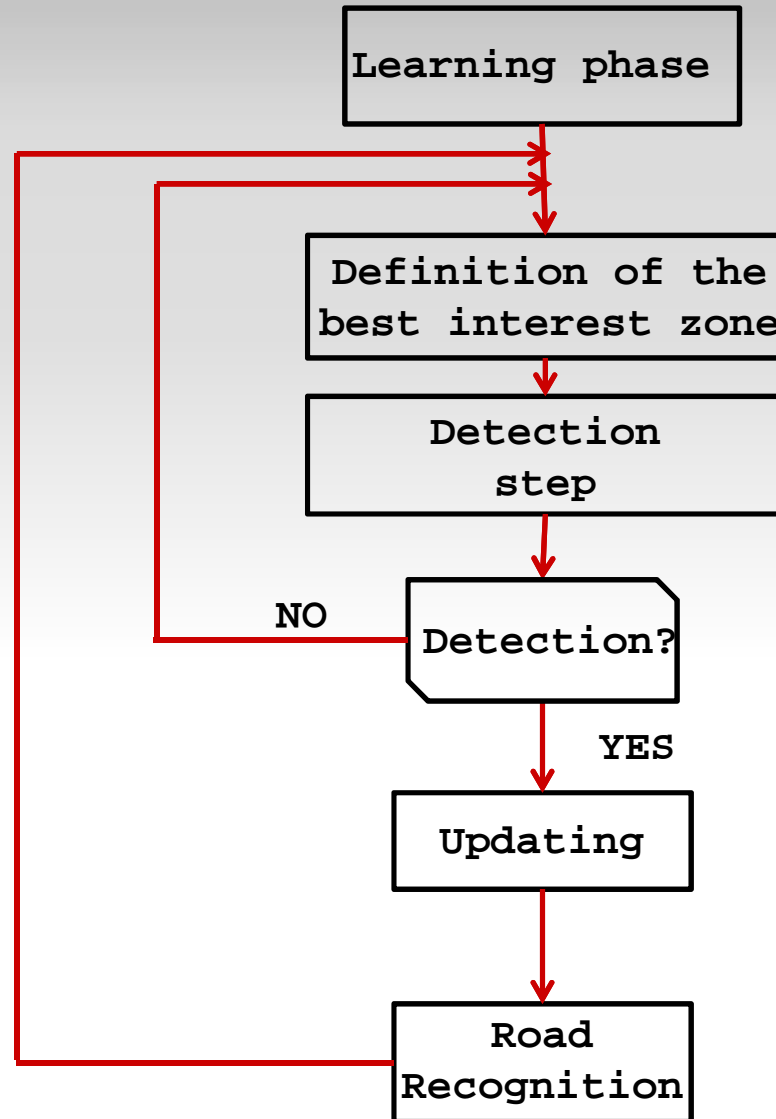
Hypothesis 3



Score of recognition 3



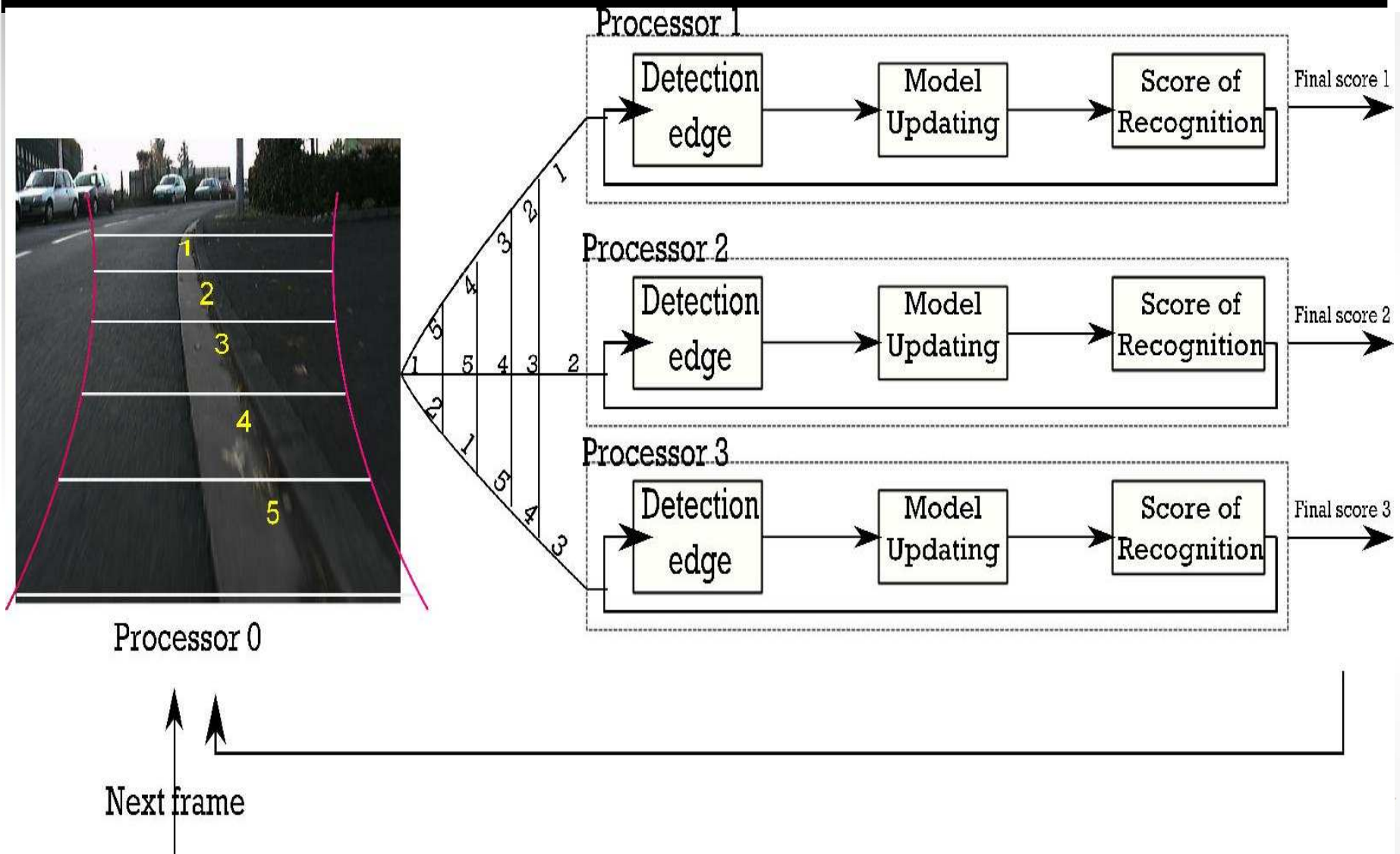
Organization chart of the recognition step



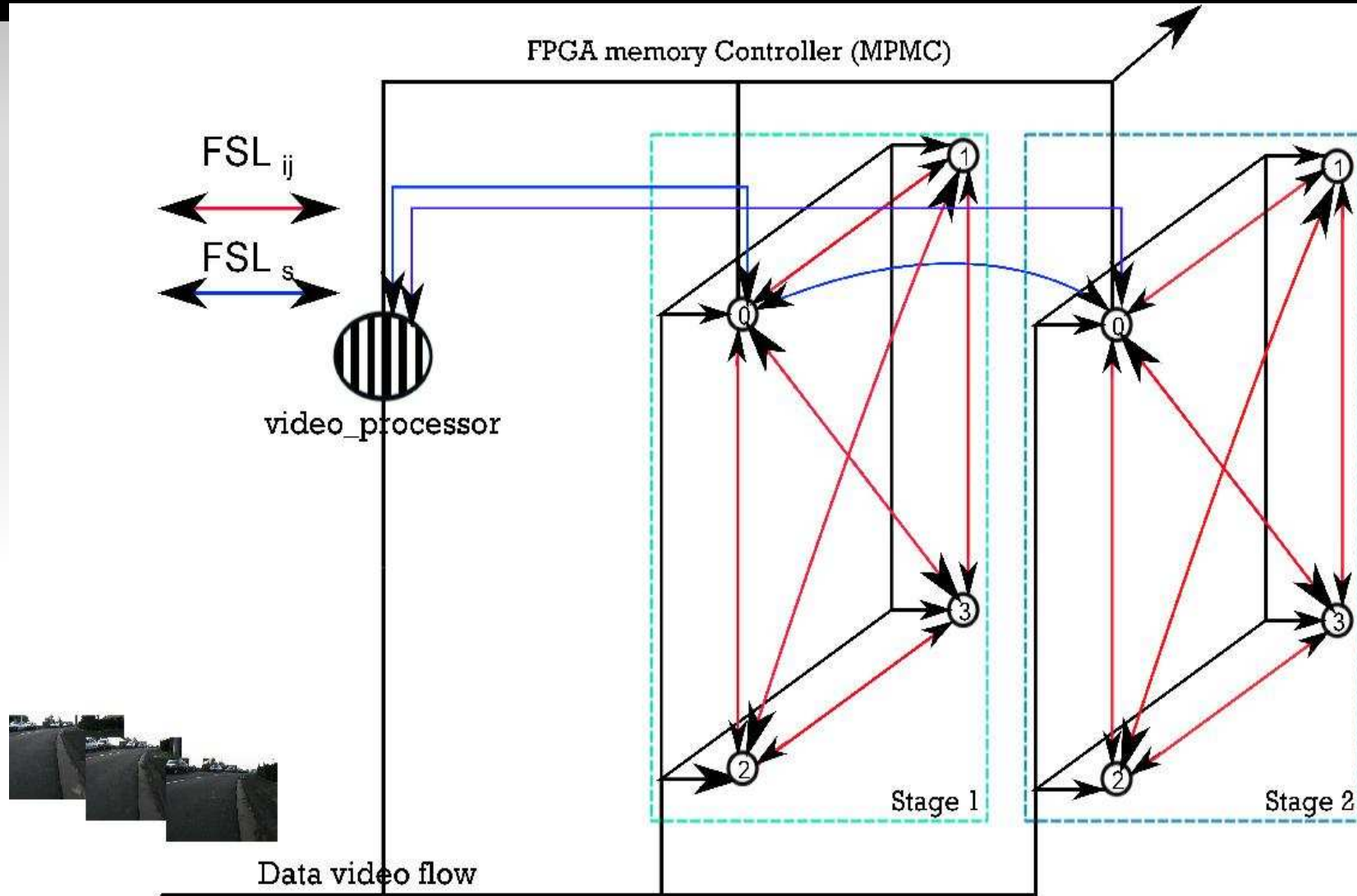
Parallel implementation of recognition algorithm



Application parallelization



Parallel architecture

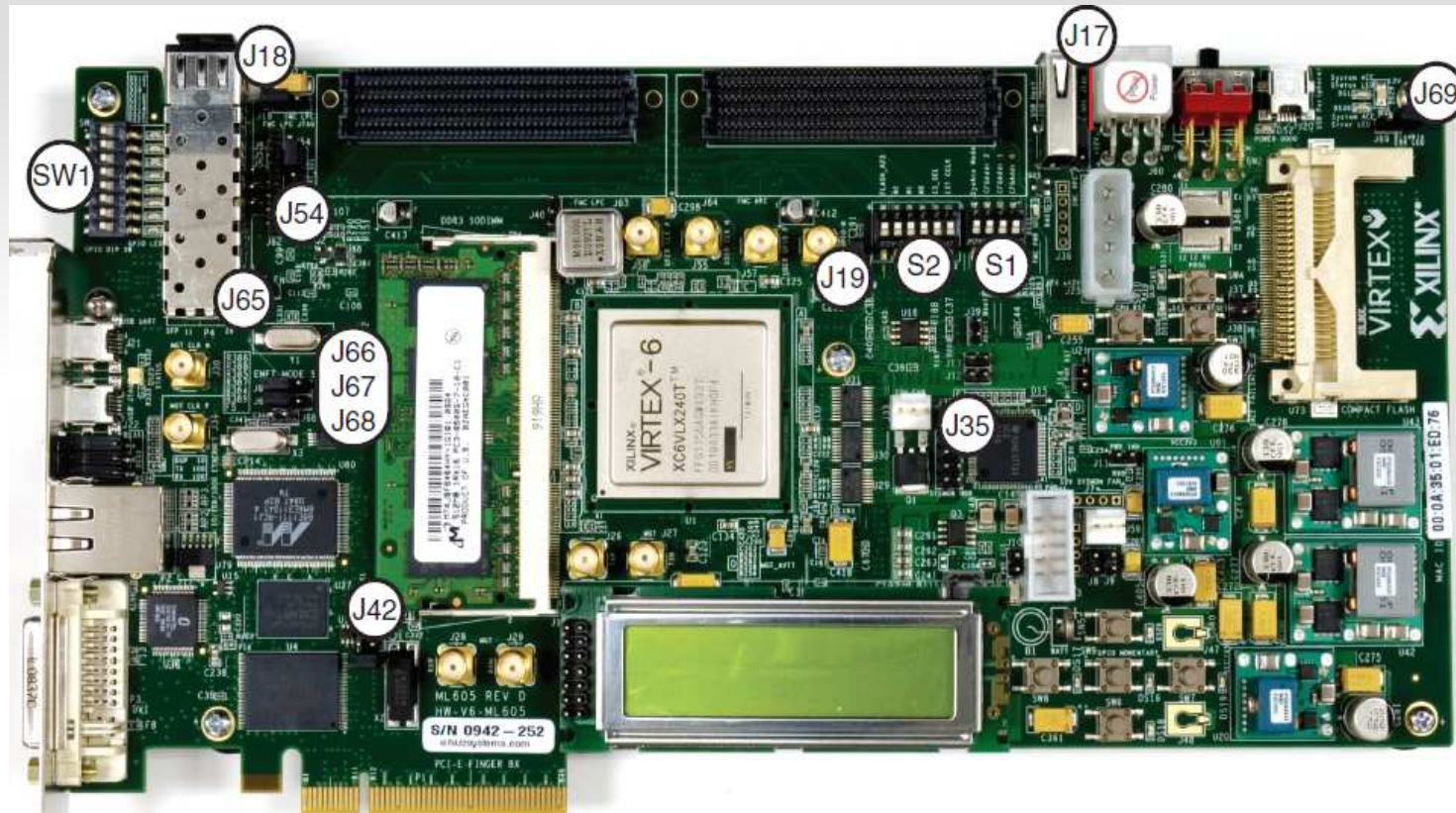


Experiments && Conclusion



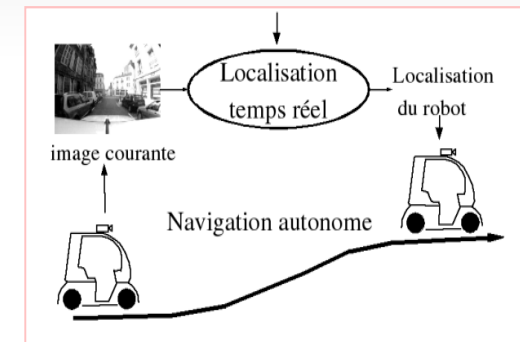
Experiments implementation

Road recognition Demo



Conclusion

- Some research of Institut Pascal groups focus their work in development of autonomous robot navigation.
- As a consequence, we propose :
 - Multi-processors approach for embedded systems.
 - HNCP methodology that allows to quickly prototypes different flavors of a given application
 - Prototypes designed in a very short time frame.
 - Prototypes validated by simulation and on board (FPGA, up to ~50 processors up to now)



Thank you!

