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Advanced Imaging S.L.

Towards Gfps CMOS image sensors

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Outline

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- **Introduction**
- **High speed CMOS**
- **Towards Gfps**

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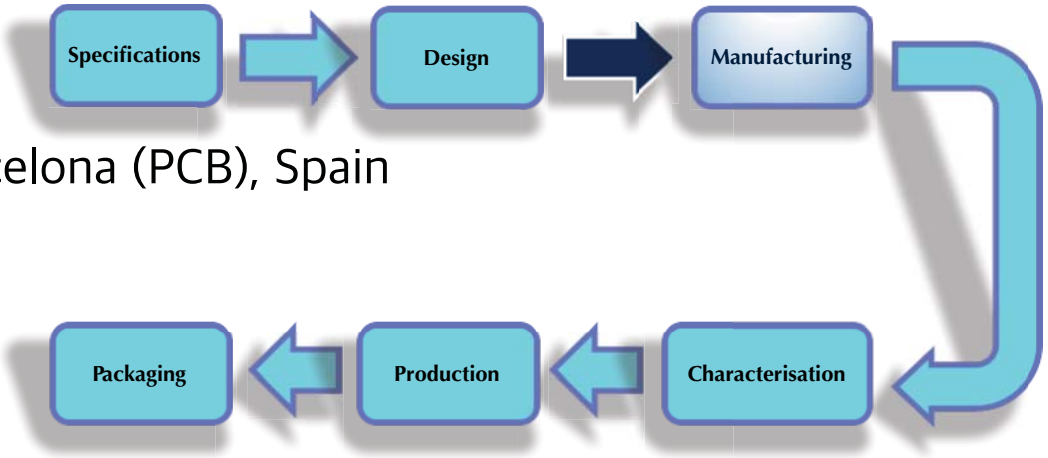
- **Introduction**
- **High speed CMOS**
- **Towards Gfps**

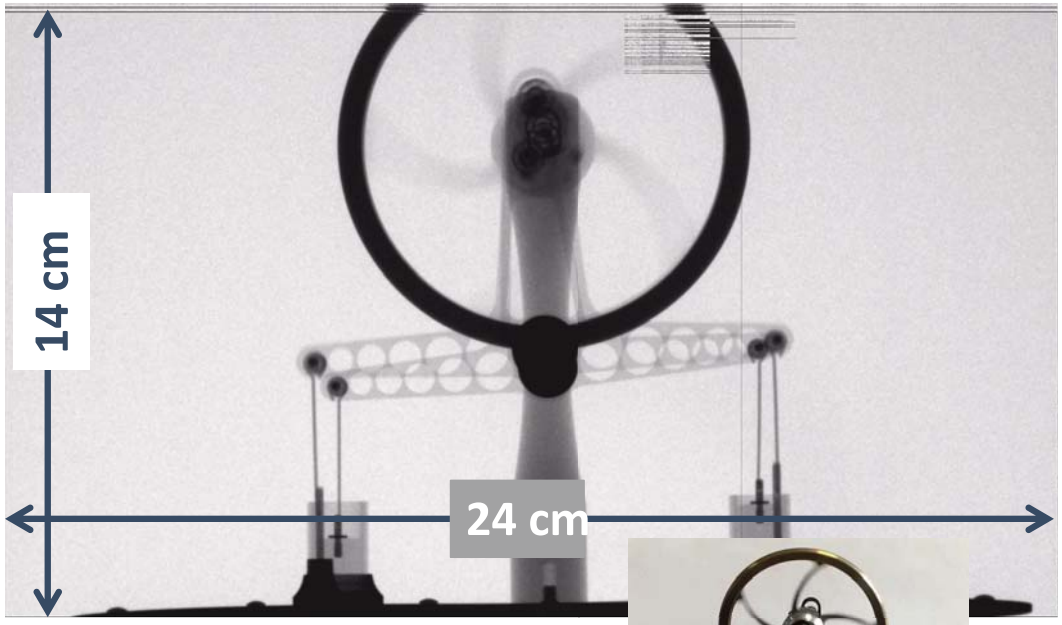
IMASENIC Advanced Imaging S.L.

- CMOS Image Sensors design house
- Developing CIS from specifications to production
- Over 40 years of cumulated experience in developing advanced CMOS Image Sensors and mixed-mode ASIC products
- Located at the Parc Cientific de Barcelona (PCB), Spain
- www.imasenic.com

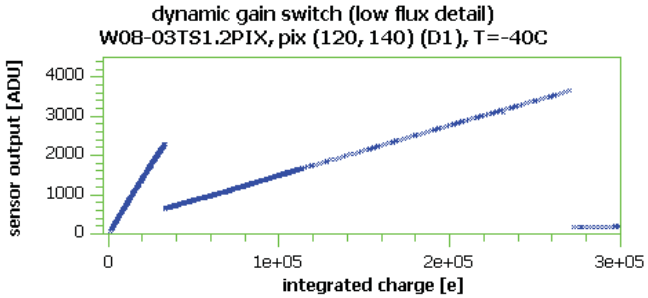


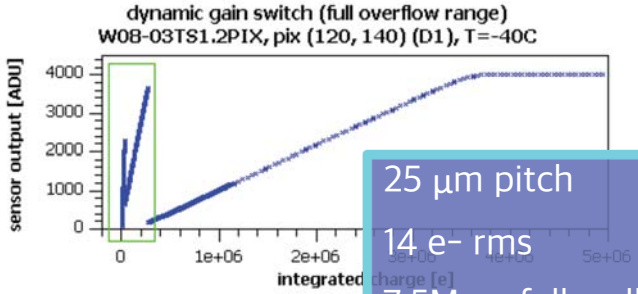
Track record. 1

- 3-side buttable, wafer-scale



- High dynamic range





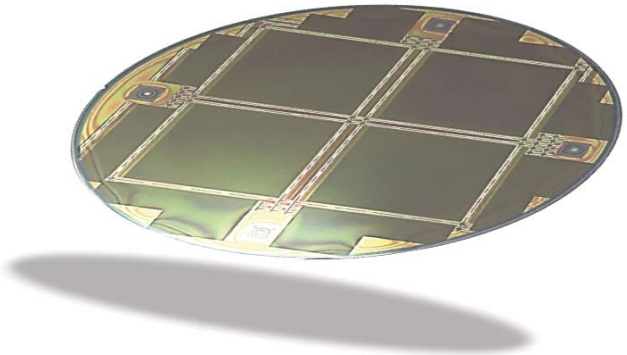
25 µm pitch

14 e- rms

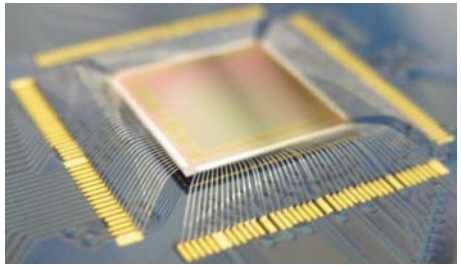
7.5M e= full well

Track record. 2

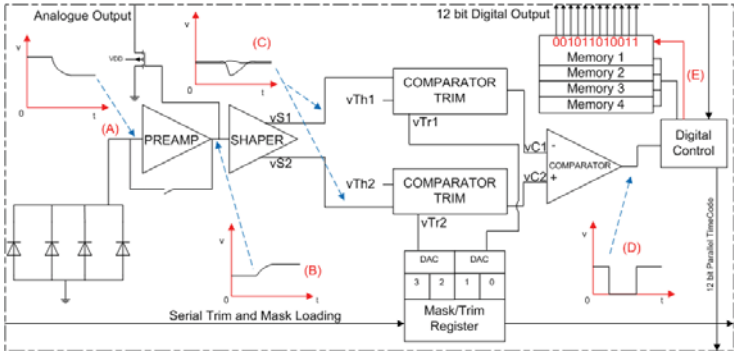
- 16Mpixel rad-hard for TEM



- Single Photon Avalanche Detectors



… and complex (smart) pixels



High/Ultra-high speed imagers

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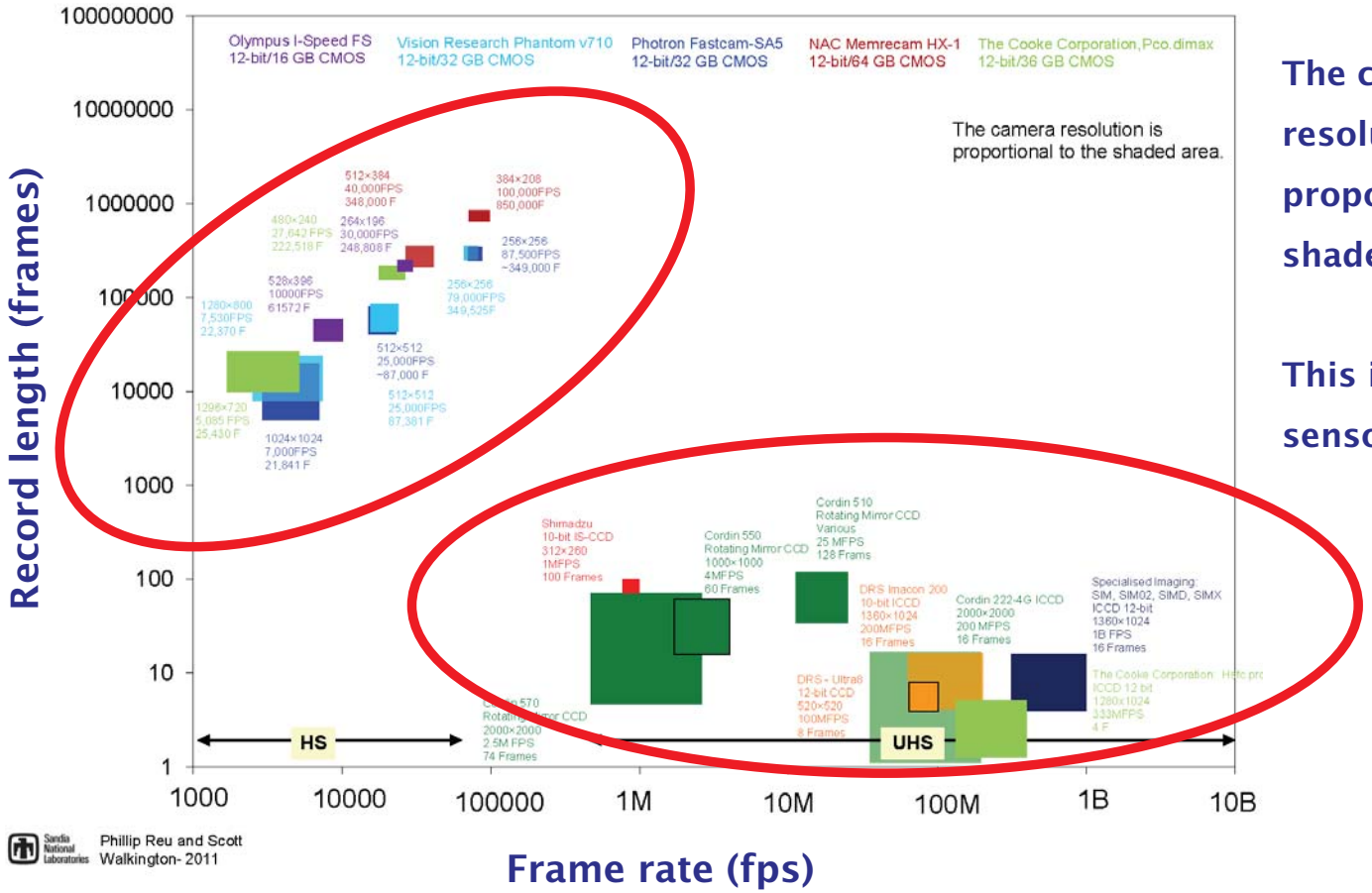

The camera resolution is proportional to the shaded area.

This is a 1Mpixel sensor

Outline

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- Introduction
- **High speed CMOS**
- Towards Gfps

Frame rate deconstructed

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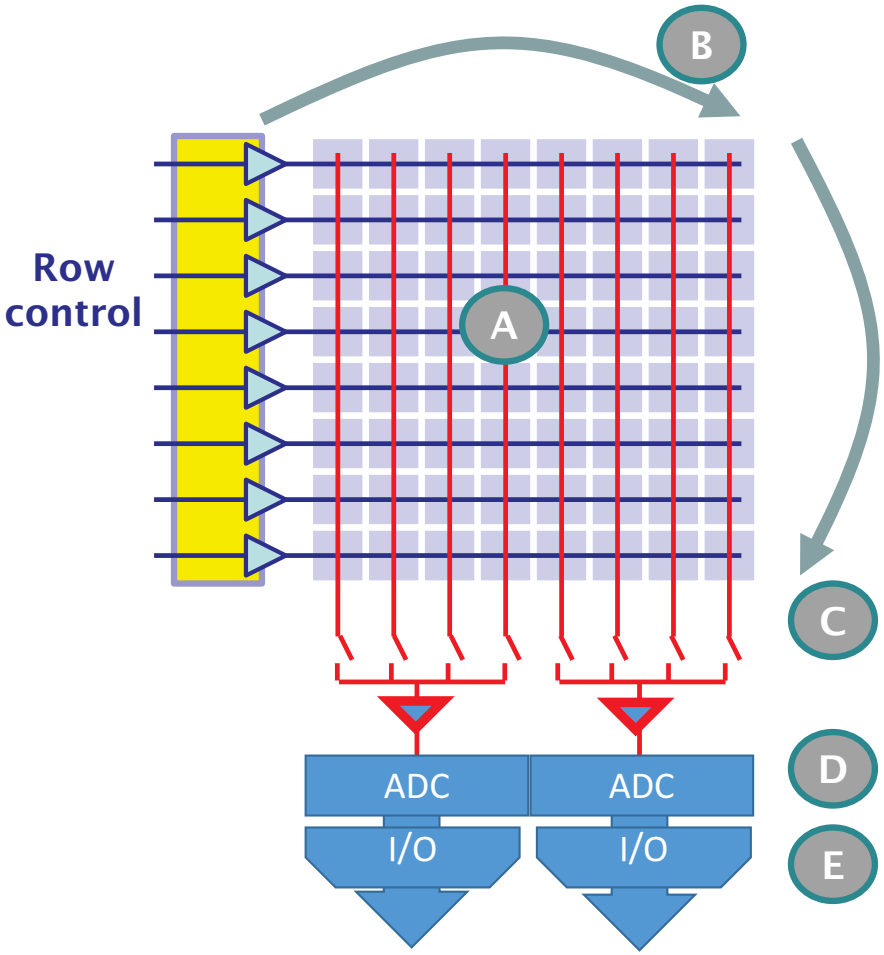
A) Charge collection

B) Time to select a row

C) Time to settle the data at the periphery

D) Analogue-to-Digital Conversion

E) I/O



ADC options

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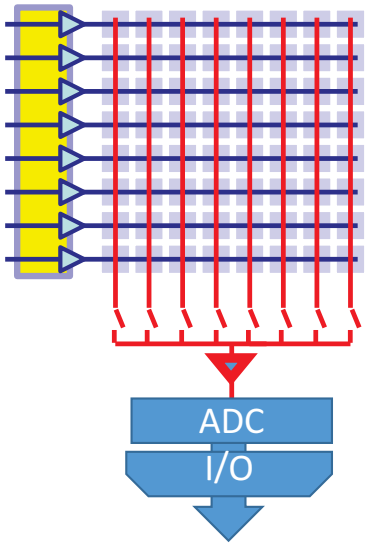
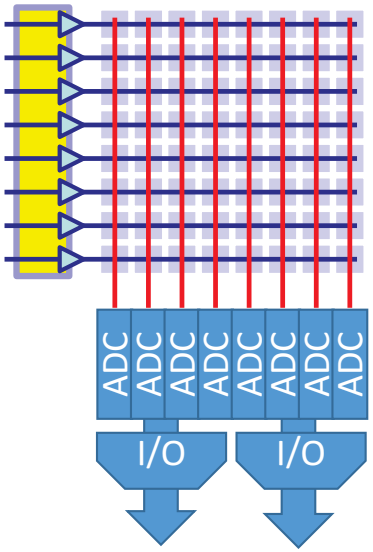
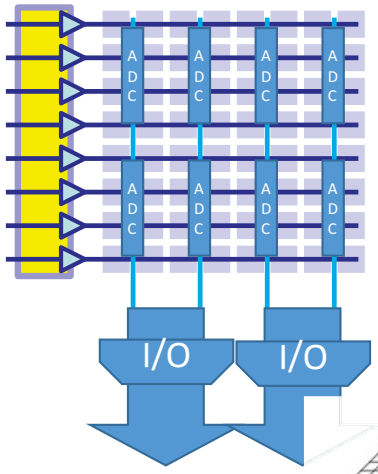
Global (chip)



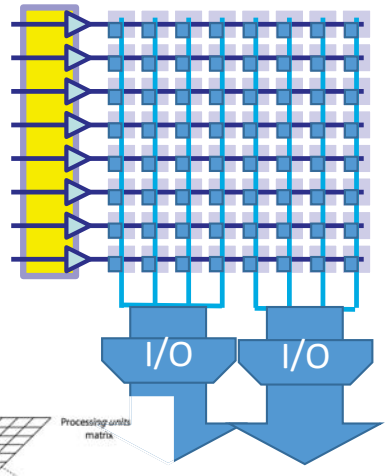
Column-parallel

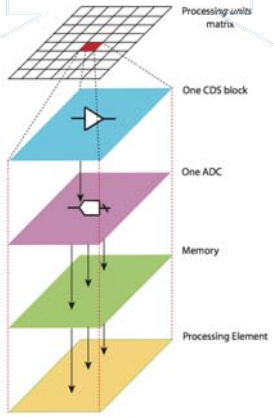


Block



Per-pixel





ADC architectures

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Figure of Merit = Noise * $(Pitch)^2$* Power/ $(2^{Nbits}*F_s)$

F_s = sampling frequency

[µJ μV_{rms} μm^2]

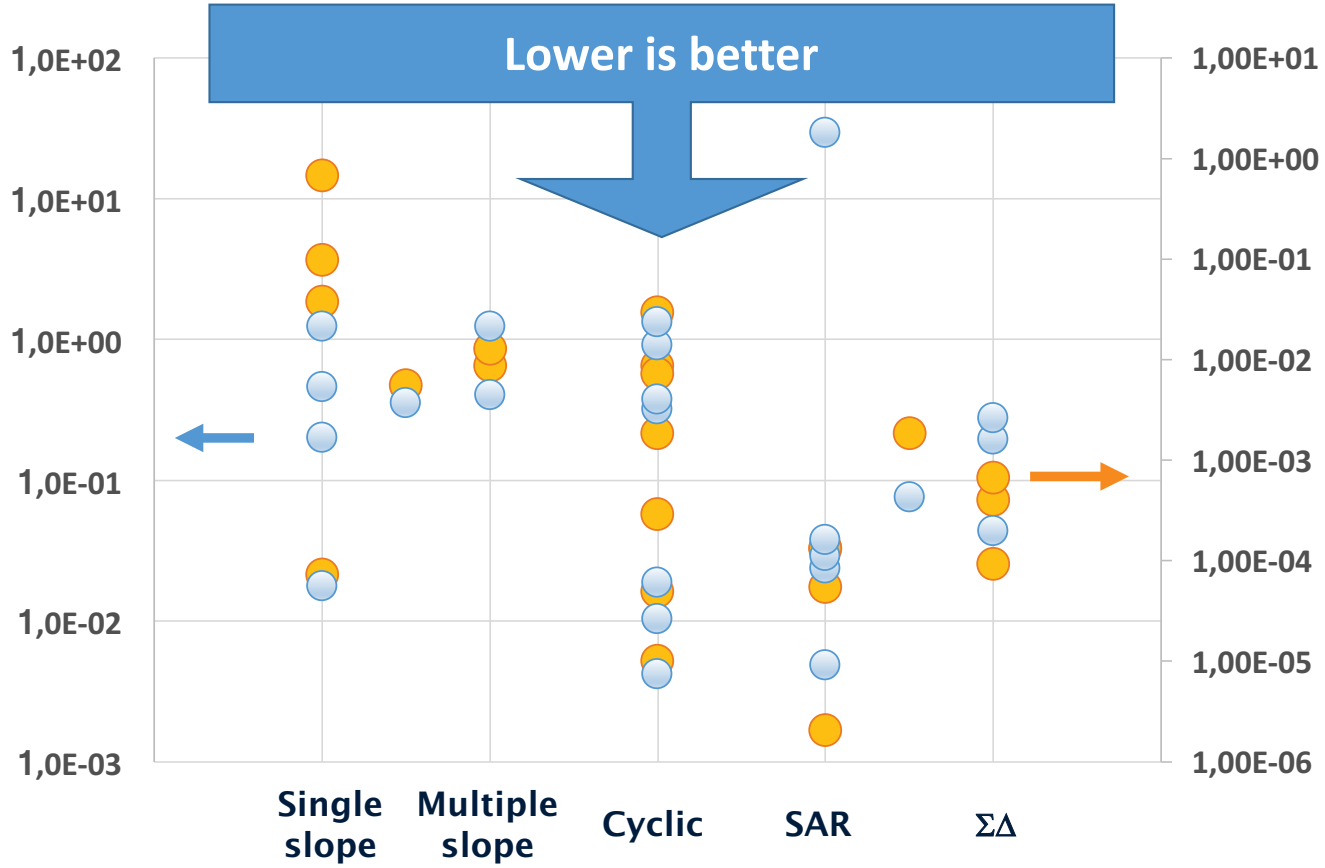

Figure of Merit = Noise * Area* Power/ $(2^{Nbits}*F_s)$

F_s = sampling frequency

[µJ μV_{rms} μm^2]

Adapted from Leñero 2016

Frame rate

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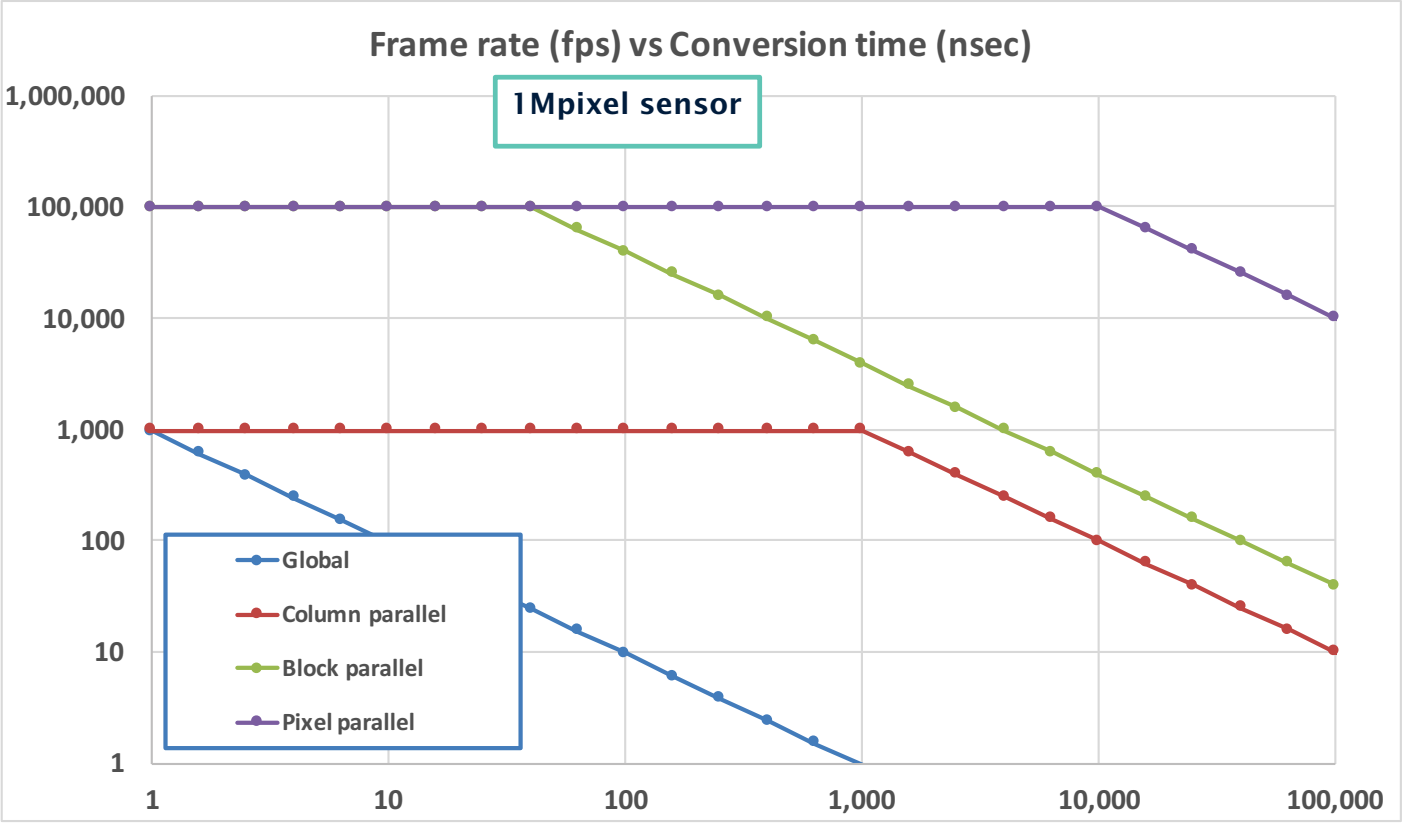


16x16 blocks

1 ADC per column

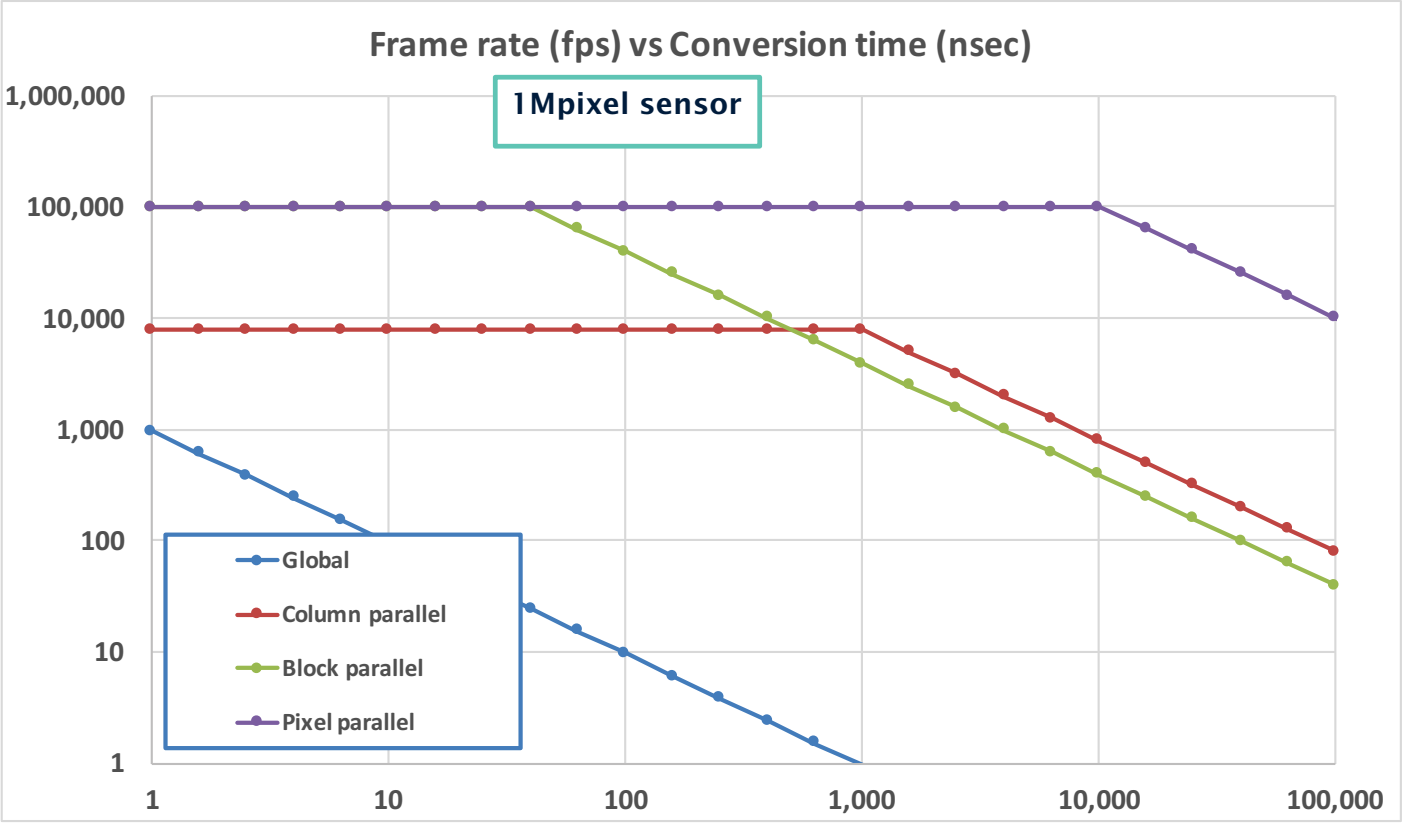
2 Gbit/sec IO

10 bit accuracy

1µsec blanking time (and proportional for block r/o)

512 IOs (10 for Global ADC)

Frame rate



16x16 blocks

8 ADCs per column

2 Gbit/sec IO

10 bit accuracy

1µsec blanking time (and proportional for block r/o)

512 IOs (10 for Global ADC)

Frame rate

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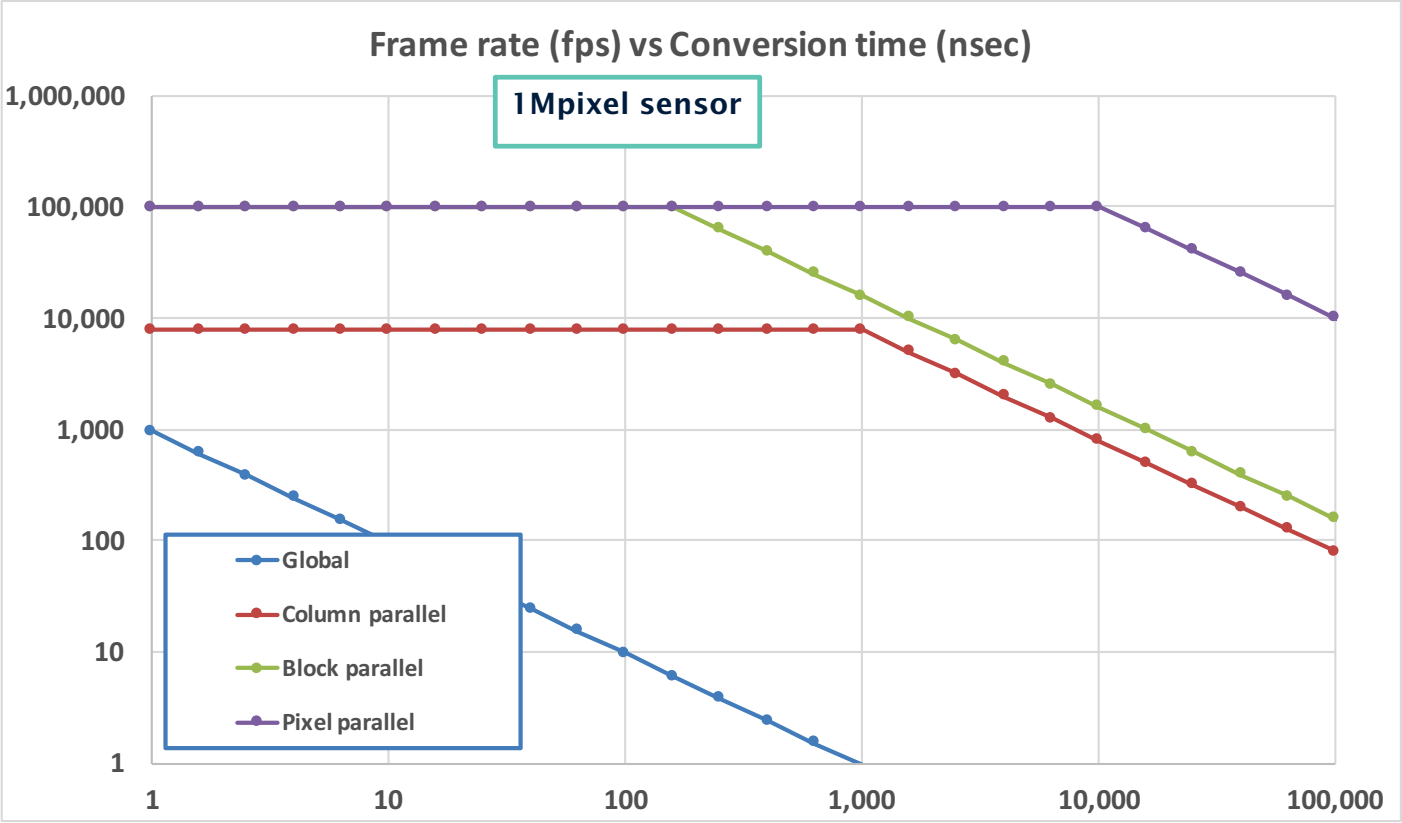

8x8 blocks

8 ADCs per column

2 Gbit/sec IO

10 bit accuracy

1µsec blanking time (and proportional for block r/o)

512 IOs (10 for Global ADC)

Frame rate

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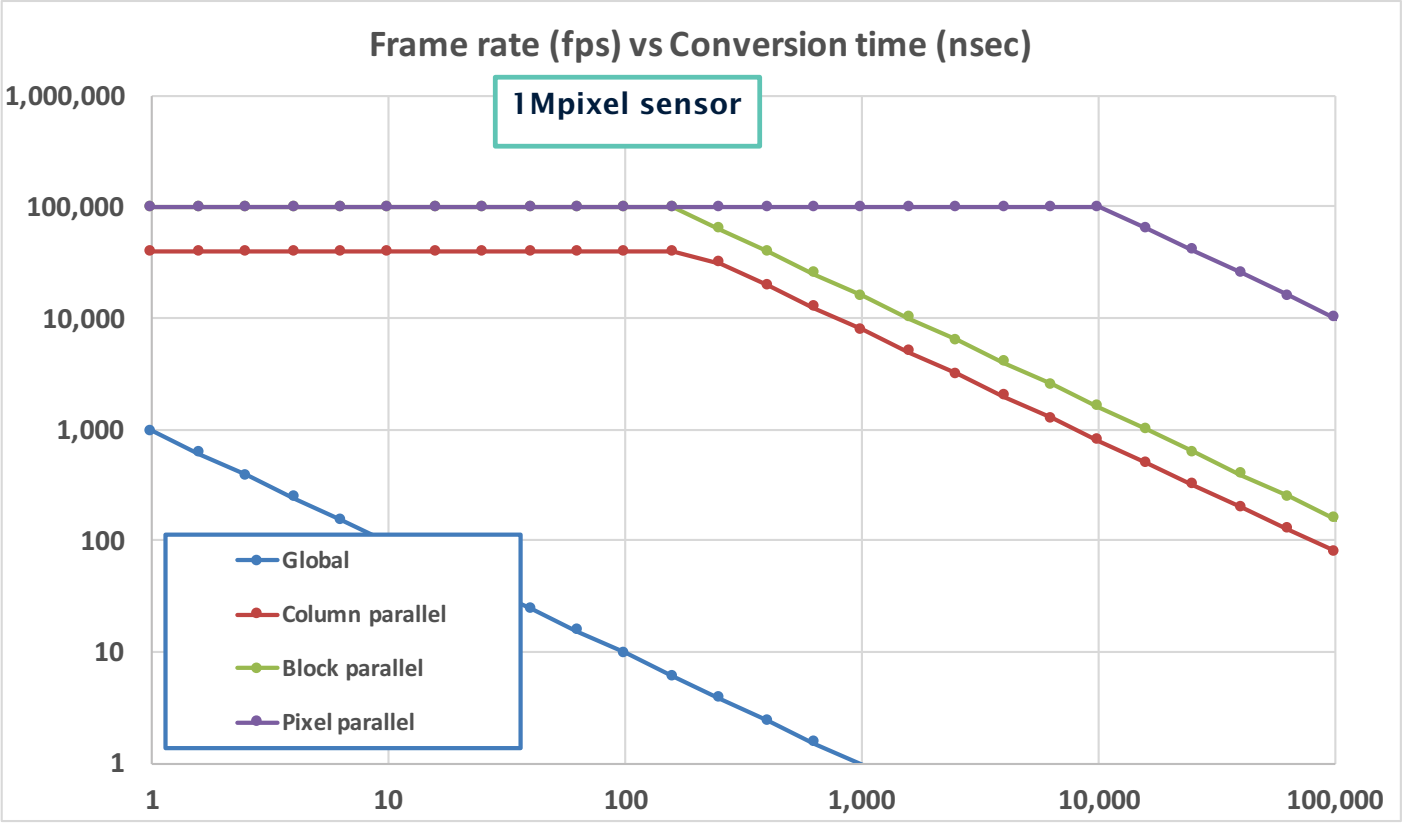

8x8 blocks

8 ADCs per column

2 Gbit/sec IO

10 bit accuracy

0.2µsec blanking time (proportional for block r/o)

512 IOs (10 for Global ADC)

Frame rate

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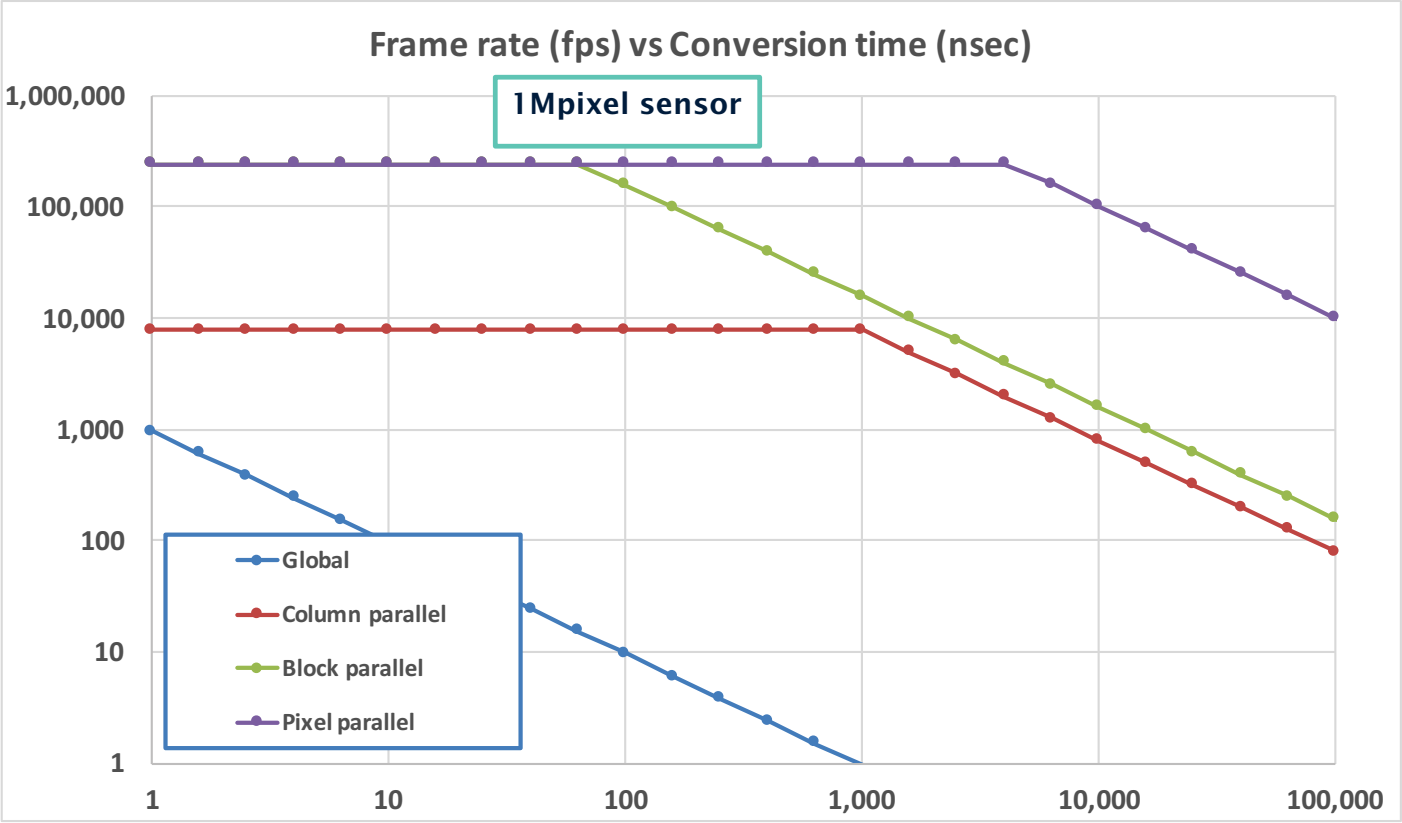

8x8 blocks

8 ADCs per column

5 Gbit/sec IO

10 bit accuracy

1µsec blanking time (and proportional for block r/o)

512 IOs (10 for Global ADC)

High-speed summary.

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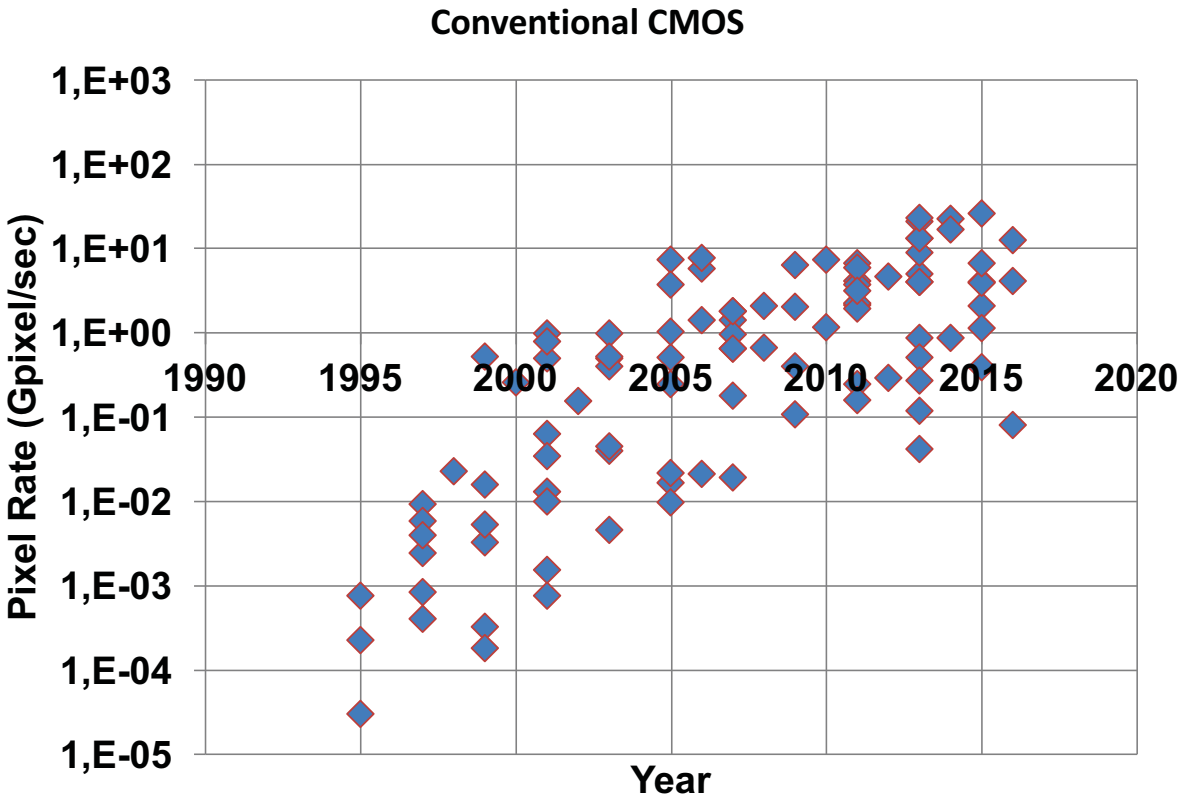

Outline

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- High speed CMOS
- Towards Gfps

Ramo-Shockley's theorem

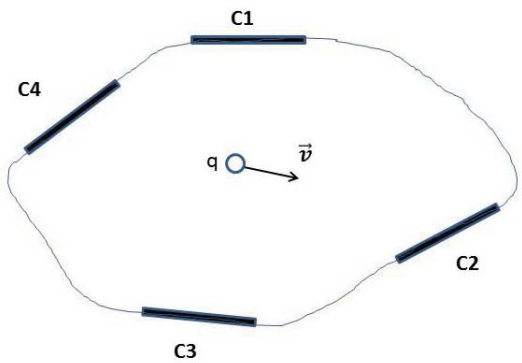
Current i(t) on one electrode due to a charge q moving with speed v(t) at point

$$i_k(t) = q\,\vec{v} \cdot \overrightarrow{E_W}$$

$E_w(x)$ is the electric field obtained by setting the selected electrode at unit potential, all other electrodes at zero potential. (Shockley 1938, Ramo 1939)

$E_w(x)$ calculated after removing all space charge .

(Cavalleri et al. 1971)

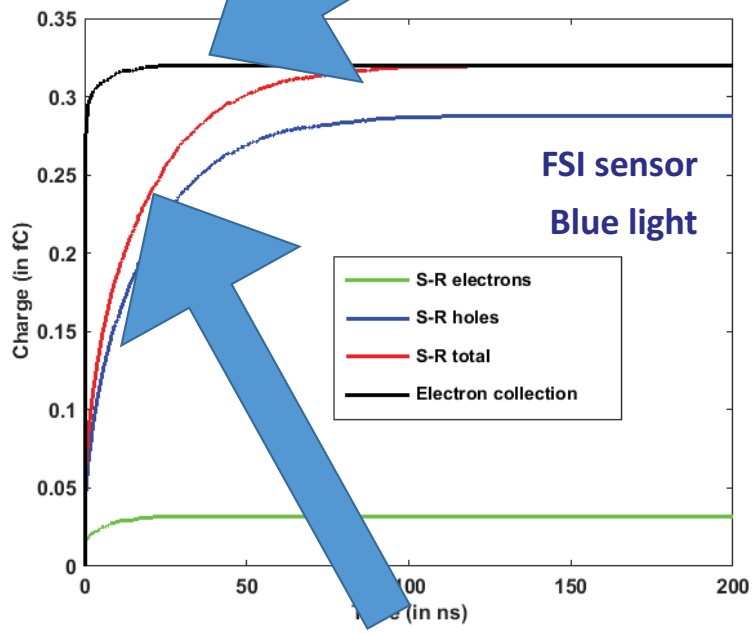


The current signal is induced by the movement of charge

Consequences

- The current signal is induced by the movement of charge
- In semiconductor there are two types of carriers, electrons and holes, hence two current components
- The two components are summed to give the total current
- The integral of the total (sum) current is equa to the collected charge

What is expected from collection time



What is predicted by Shockley-Ramo

Temporal colour cross-talk

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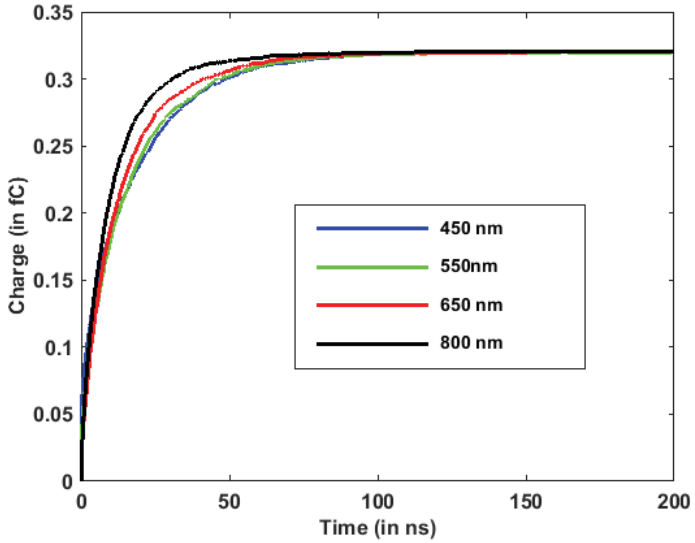
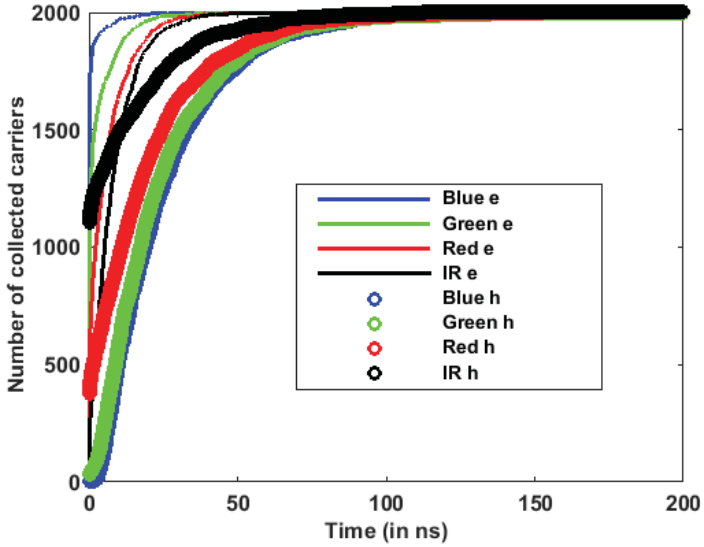
Ramo-Shockley



Carrier collection



Thin epi. Low resistivity.

Overbias on a 12µm thick epi

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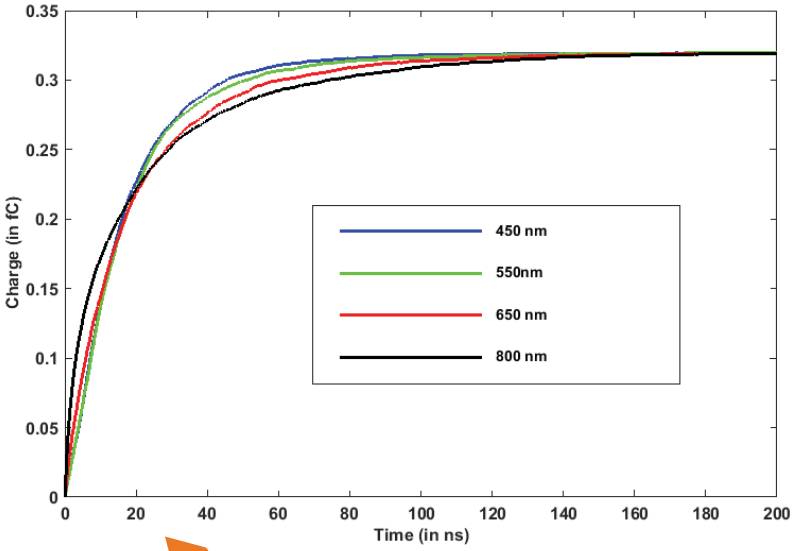
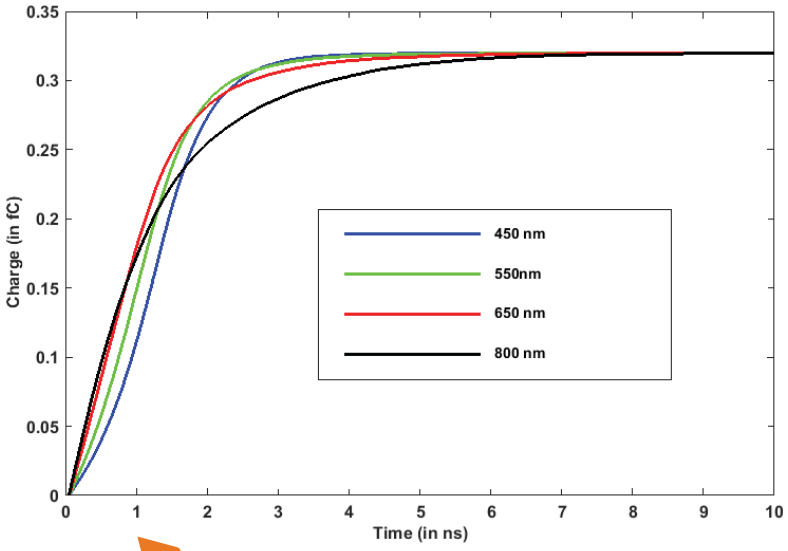
V_{bias} = 1.5V



20 ns

V_{bias} = 5V



1 ns

Sub-ns collection time > Gfps frame rate

What about photon counting ?

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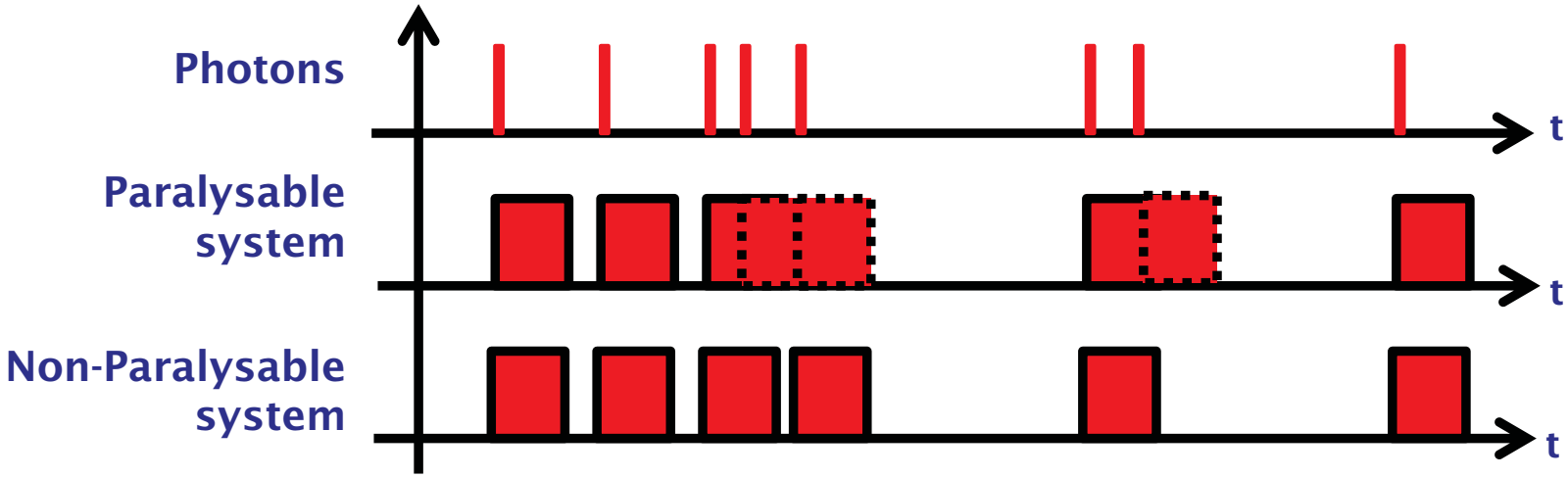
Deadtime in counting systems. Basic models: paralysable and non-paralysable



Counting curves

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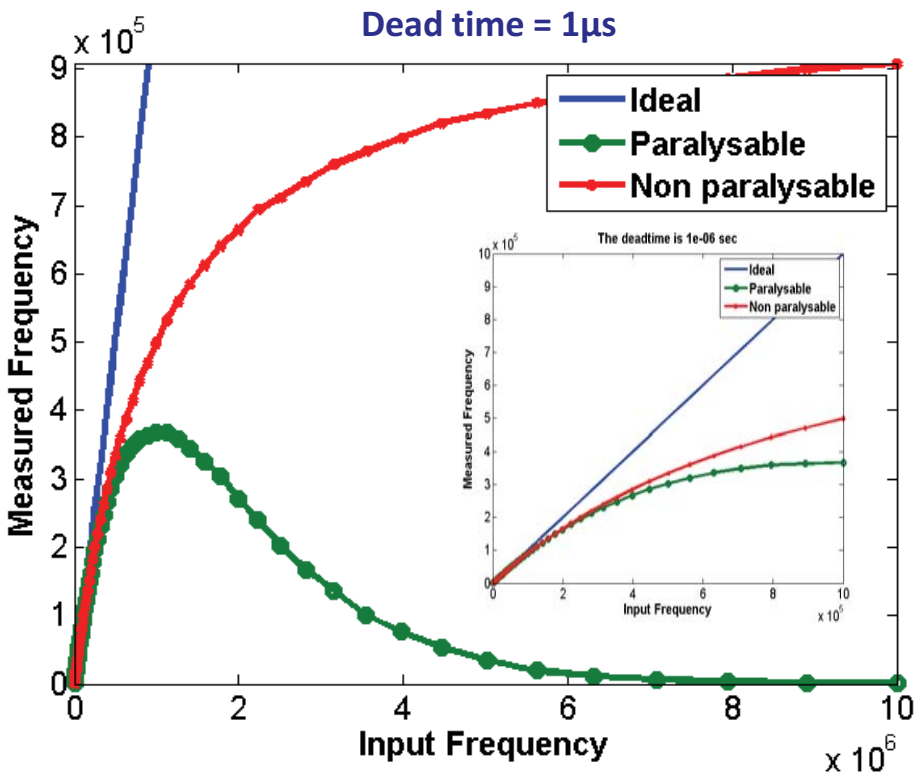
Maximum count rate set by dead time

Linear counting rate ~ 1 / (10 * deadtime)

Frame rate ↑↓

Maximum count ↓↓

Bit depth



Practical implementation

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Towards Gfps

A) Time stamping (photon counting)

B) Time Pixel Multiplexing

C) Burst (framing) image sensors

Time stamping

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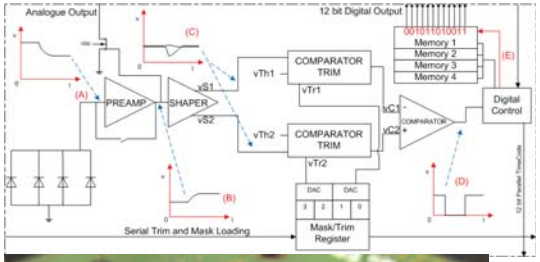
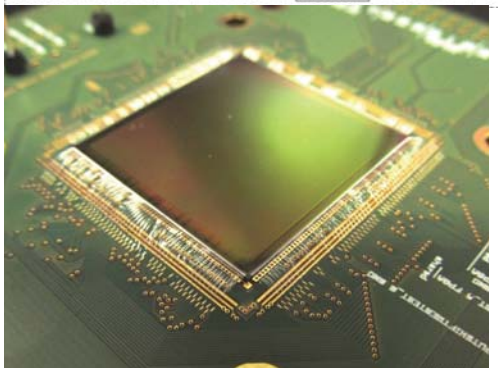
In-pixel signal conditioning





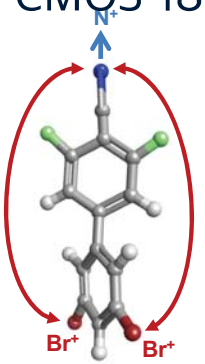
PImMS

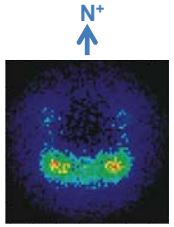
388x388

Standard diodes

Timing resolution (12.5 ns)

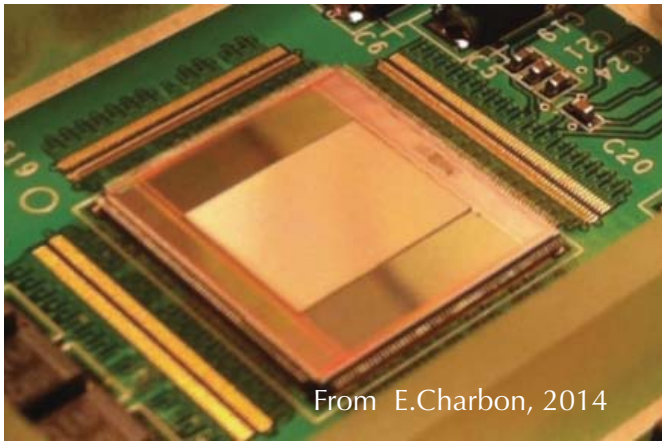
CMOS 180 nm





Single-photon Avalanche detectors (SPAD)

Megaframe

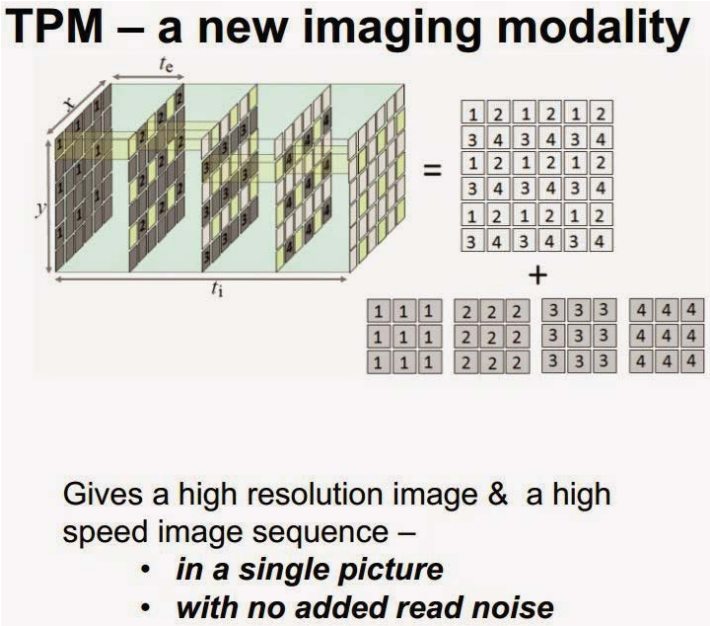


160x128 SPAD

Timing resolution (119 ps FWHM)

CMOS 130 nm

Time Pixel Multiplexing



Courtesy of G. Bub, Oxford University, 2016

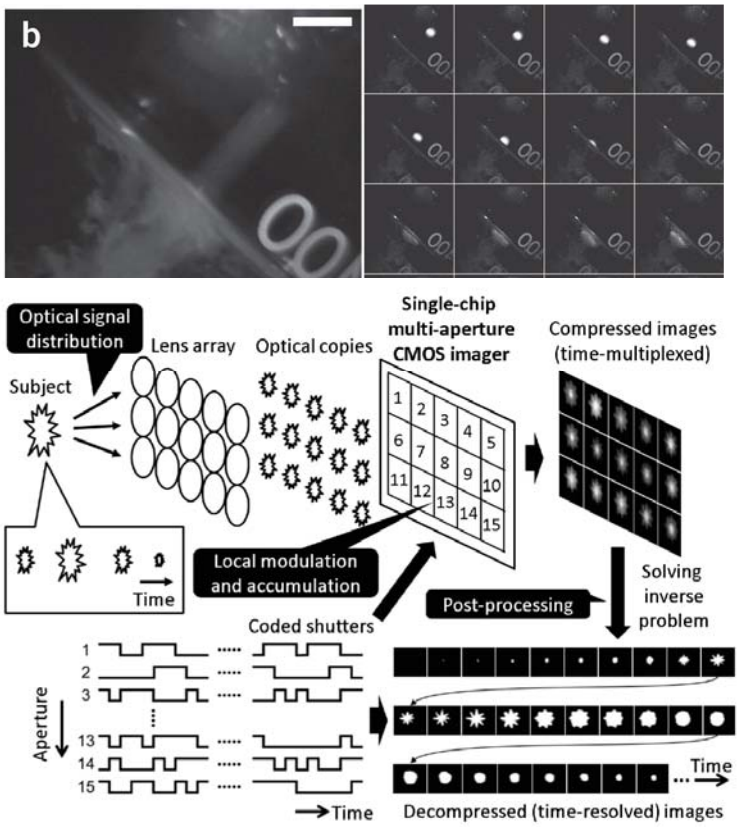


Figure 6.4.1: Overall flow of image acquisition and reproduction with a multi-aperture single-chip CMOS imager.

High resolution still picture acquired to a lower resolution, high-speed video

Conventional camera used together with Digital Micromirror Devices (DMD)

Multiple sensors on same substrate

F. Mochizuki et al., ISSCC 2015

Burst (framing) sensors

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On-chip storage

A) Voltage storage

Sample voltage on capacitor

B) Charge storage

Charge is stored and transferred to readout node

Voltage mode

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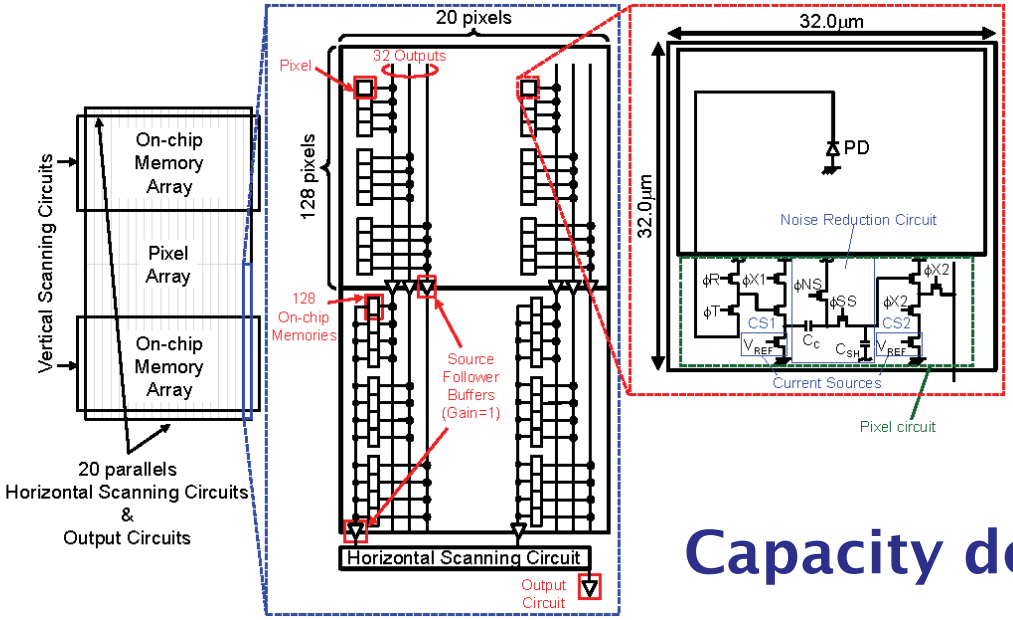
On-chip storage

'Brute force'

global shutter

Data stored in periphery



Tochigi, 2013

Capacity density sets the limit to in-pixel storage

Charges in the diode

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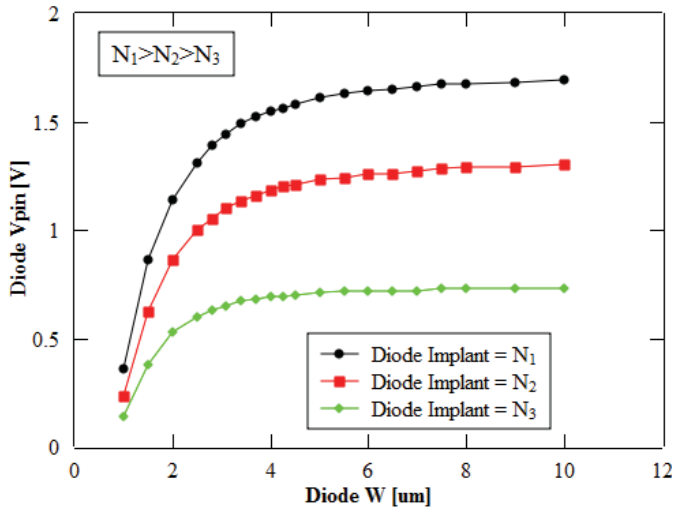
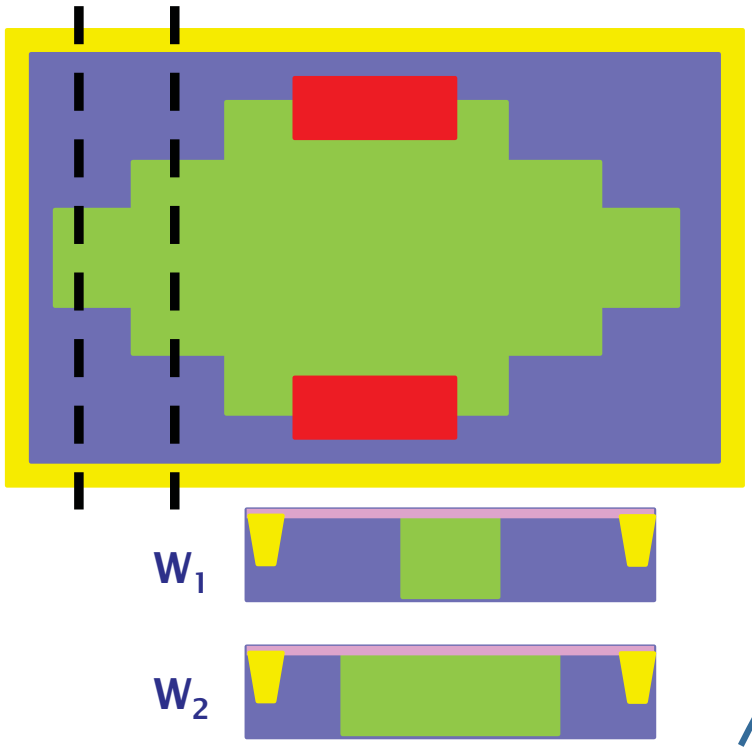
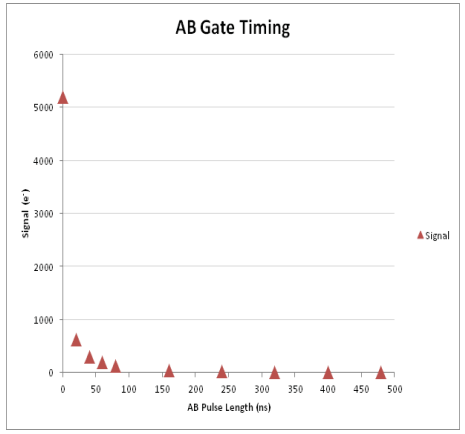
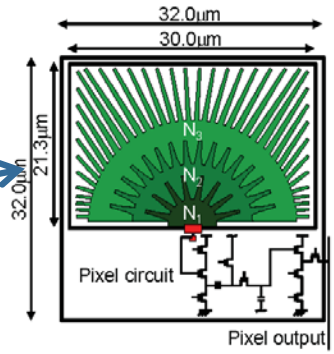
'W effect'



Lahav 2013







Miyauchi, 2014

Charge storage

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CCD-in-CMOS

Tower 180 nm

CIS

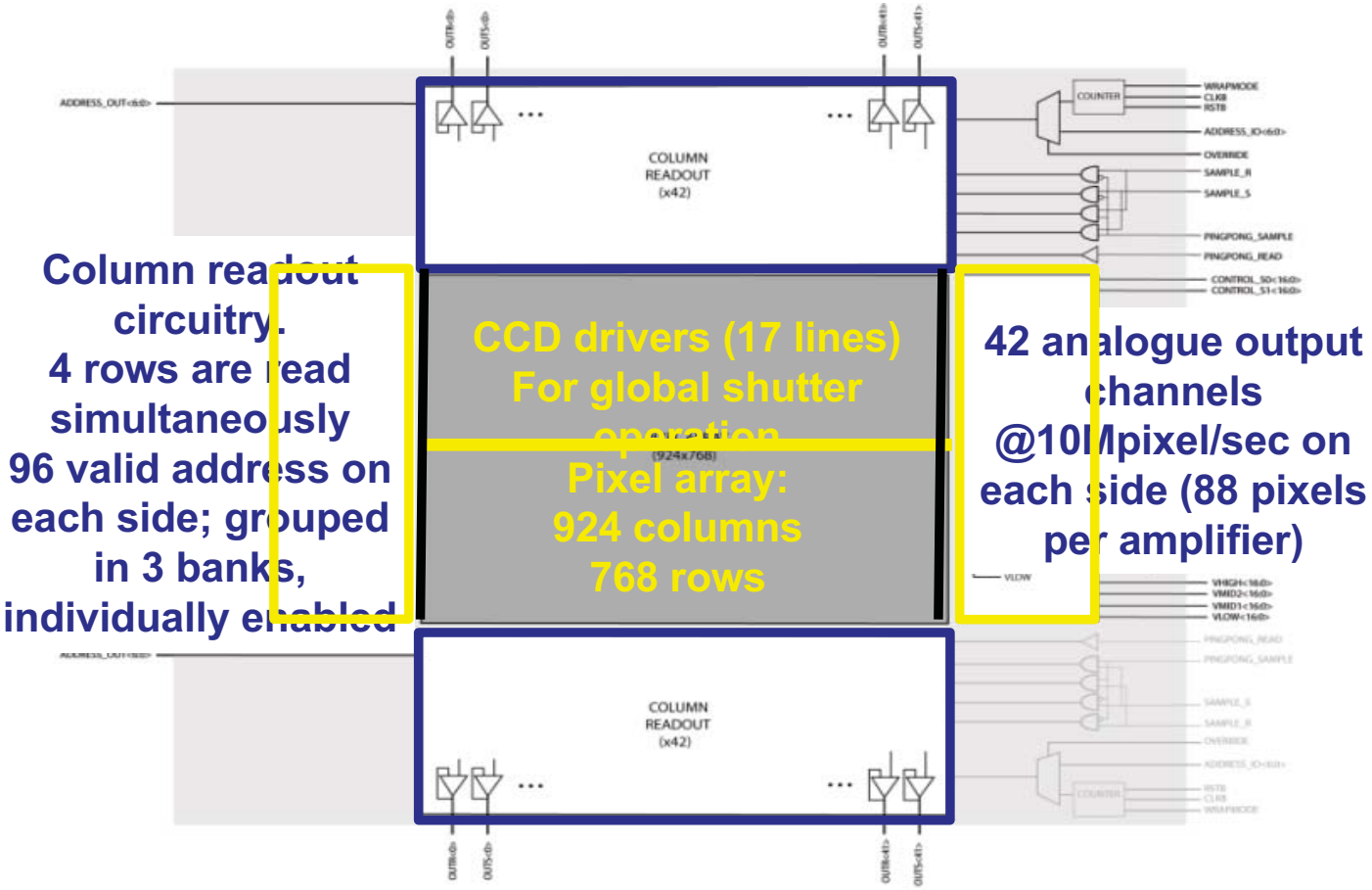
CCD module

developed for

the frame

storage, in the

pixel



Kirana pixel

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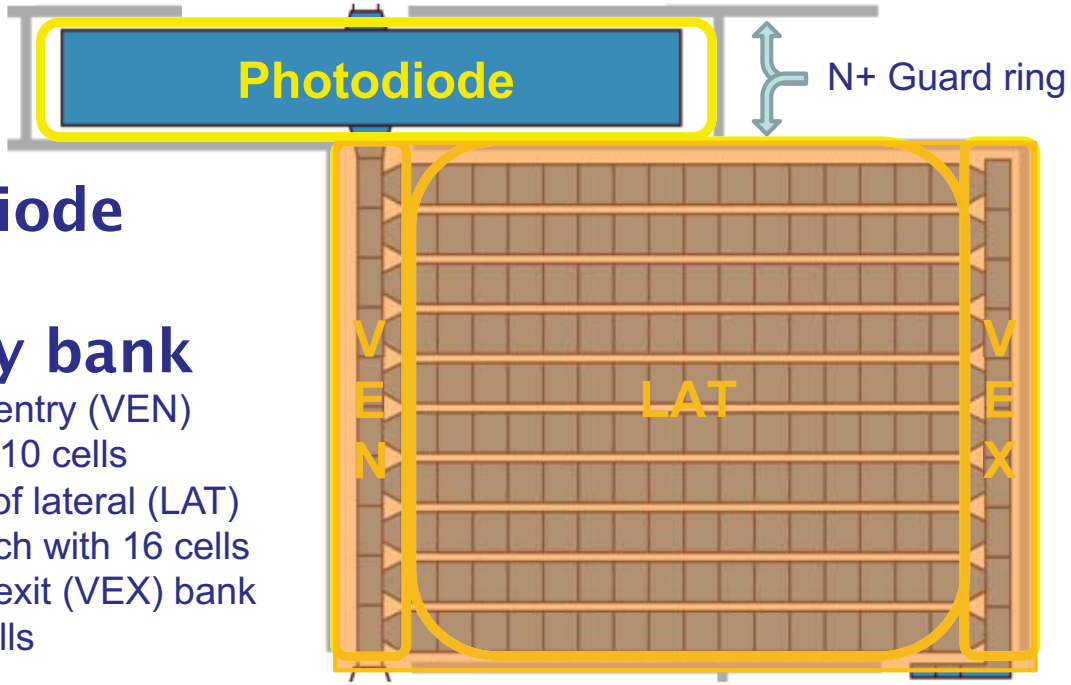
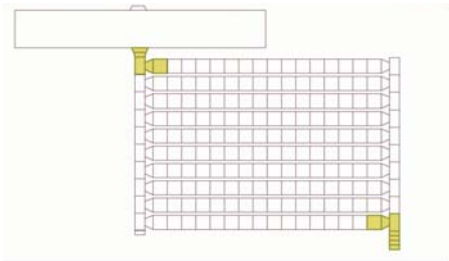
Photodiode

Memory bank

- A vertical entry (VEN) bank with 10 cells
- Ten rows of lateral (LAT) banks, each with 16 cells
- A vertical exit (VEX) bank with 10 cells





Kirana array

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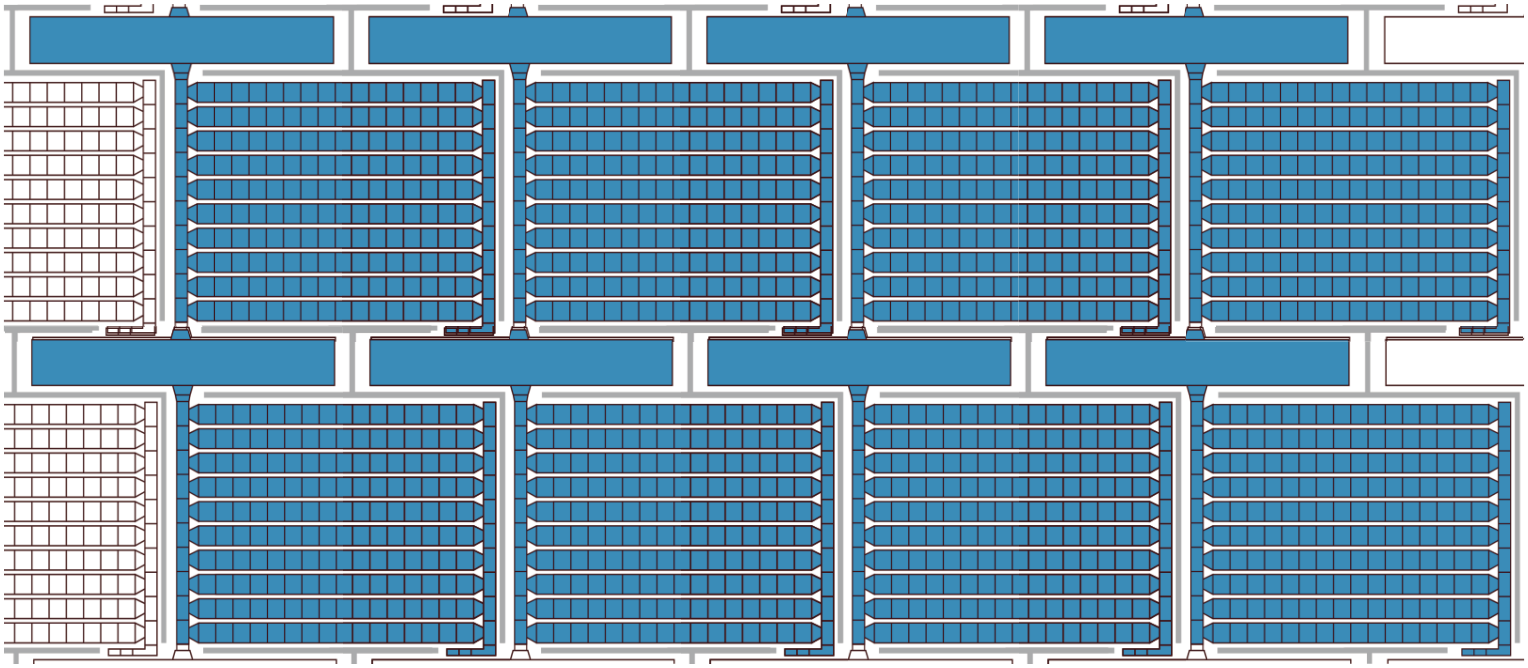

Highly scalable architecture:

- **Number of memory cells**
- **Number of pixels**
- **In-pixel storage: minimal load**
- **Low power**

Kirana improvements

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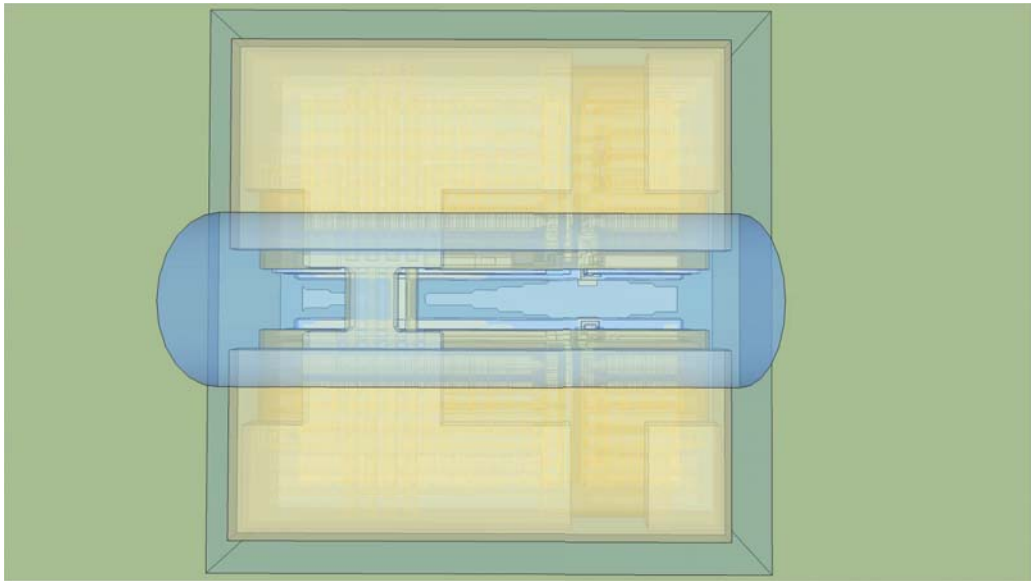

A) Microlenses for improved sensitivity: 2.5 improvement

B) High-resistivity wafers for faster collection time

C) Optical shielding of the memory cells

D) Improved implants for electrical shielding of the memory cell

Electronic shutter efficiency

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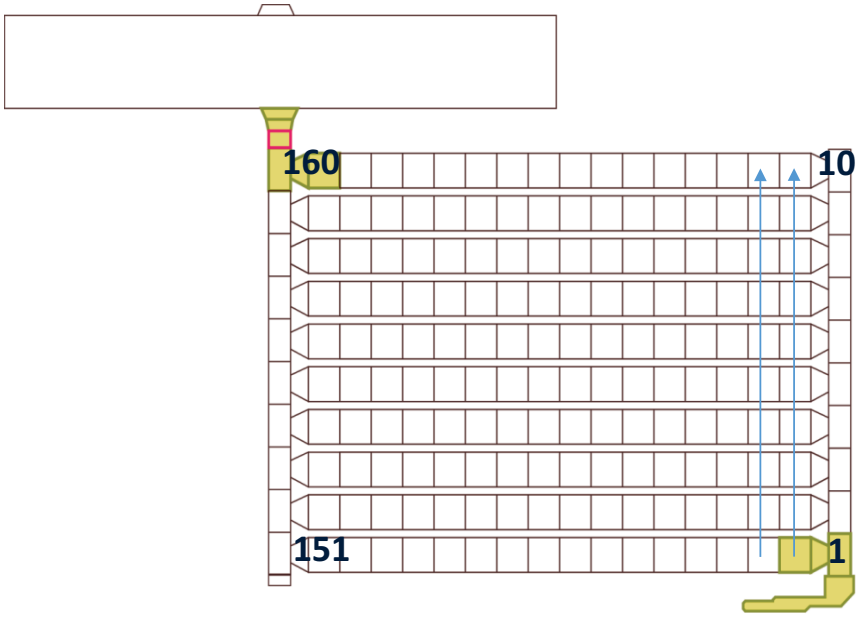

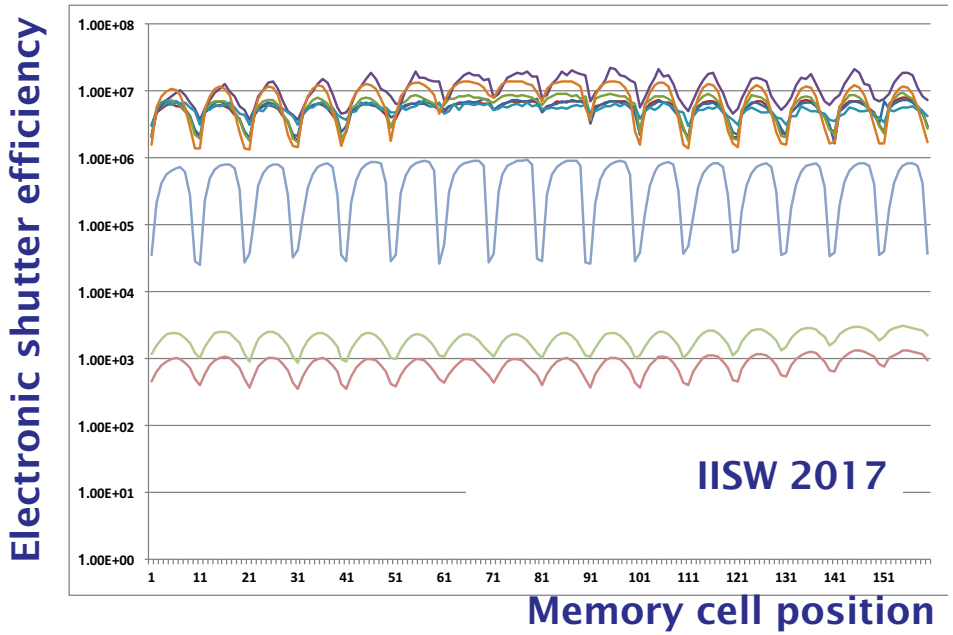

Electronic shutter efficiency > 10^7

In excess of 1,000 improvement with respect to the first sensors (presented at IISW 2013)

Ultra high-speed summary

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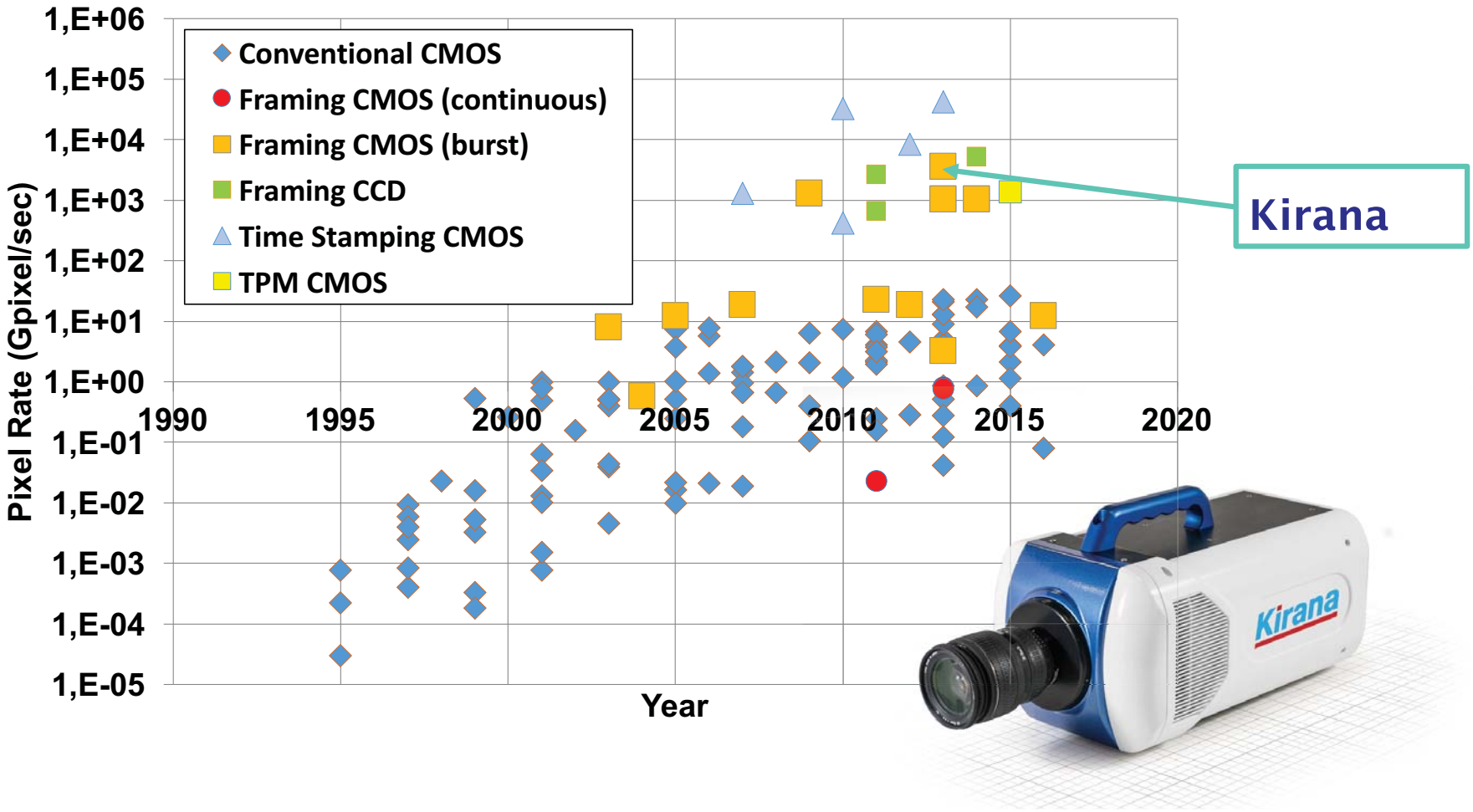

Conclusions

- Continuous frame rate. State of the art > 10Gpixel/sec

→ > 100Gpixel/sec, i.e. 100kfps @ 1Mpixel

- Sensors for Gfps: time stamping, time pixel multiplexing, burst mode sensors
- Burst mode technologies : charge and voltage sampling
- Burst mode. State of the art > Tpixel/sec, i.e. >Mfps @ 1Mpixel
- Ultimate limit from charge movement → 10-100 Gfps
- High density capacitance and 3D stacking can help

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Thank you!

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